Report of INAE Workshop
Oct. 31- Nov. 1, 2009, IIC, New Delhi

Making India Powerhouse for Semiconductor Design

Organized by:

Indian National Academy of Engineering

in association with:

Inspired, Integrated Initiative

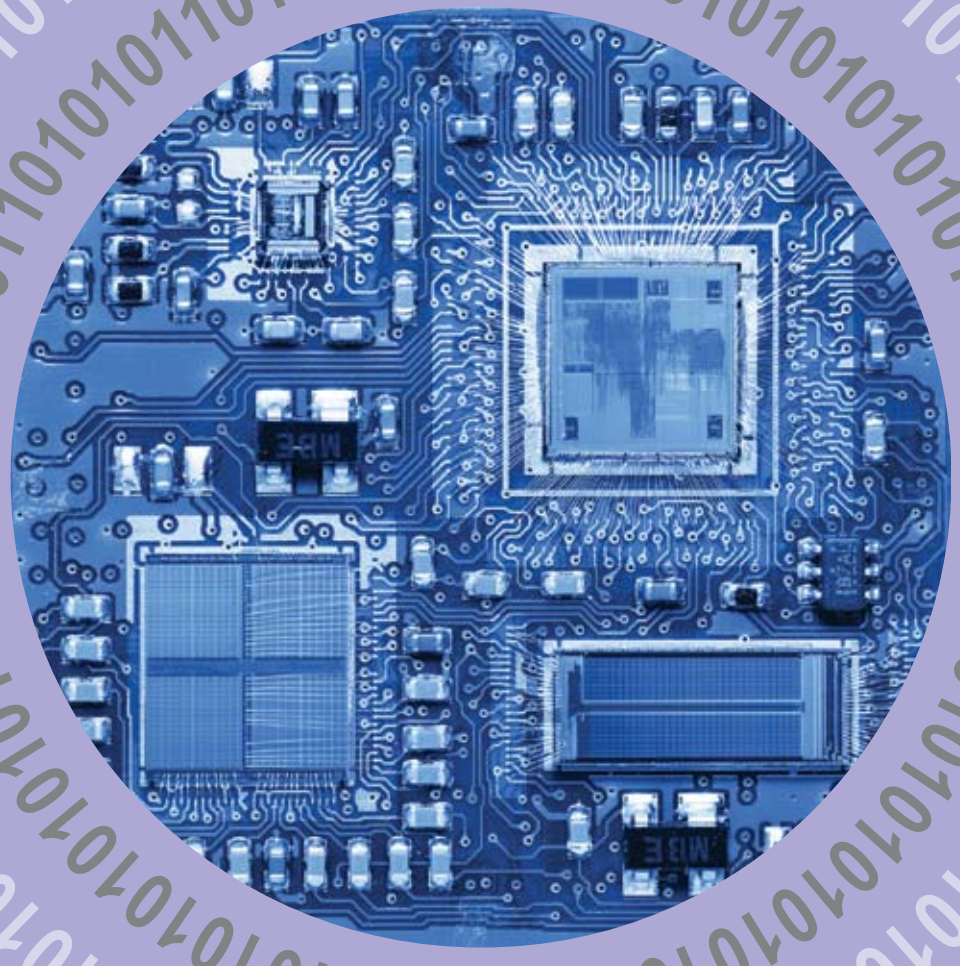
ISA INDIA SEMICONDUCTOR ASSOCIATION

India Semiconductor Association

Supported by:
Office of the Principal Scientific Advisor to the Govt. of India
Department of Information Technology, Govt. of India

Contents

Making India Powerhouse for Semiconductor Design



Preface

India is home to many semiconductor design companies, Indian as well as MNCs. The very presence of EDA, embedded system and design service companies has enriched the ecosystem. Government of India has lately been contemplating on embarking on a program for a home-grown microprocessor suitable for strategic requirements. There is an international perception that India can be as much a design hub for semiconductor products as China is in manufacturing. Therefore, notwithstanding our slow progress on VLSI fabrication/manufacturing, should we not strive to make India a real powerhouse in VLSI design? This is intended to be both in terms of all-round expertise and increased output, given that we already have made a substantial headway in this arena and have most of the key constituents in place. If such a goal has be achieved, the stakeholders from industry, government and academia have to analyze the opportunities, technical challenges, roadblocks etc. and set a realistic roadmap.

It is in this context that Indian National Academy of Engineering (INAE), in association with India Semiconductor Association (ISA) and supported by Department of Information Technology (DIT) and Office of the Principal Scientific Advisor to the Government of India, organized a workshop on the theme of 'Making India Powerhouse for Semiconductor Design' on 31 Oct-01 Nov, 2009. The workshop was attended by about fifty specialists and thought leaders in the field from industry, R&D and academia. The congregation deliberated on issues related to India's capabilities---strengths and areas of improvement in the sphere of semiconductor design. This compendium captures deliberations at the workshop and makes certain observations and actionable recommendations for giving semiconductor design in India a collective thrust.

Dr. Aloknath De
Prof. AB Bhattacharyya
Dr. MJ Zarabi

Workshop Schedule

31st October, 2009 (Saturday)

10:45—11:15: Assembly

11:15—12:00: Inaugural Session

- Objective of the Workshop by Dr. M.J.Zarabi, Vice President, INAE
- Address by Ms. Poornima Shenoy, President, ISA
- Address by Dr. P.S.Goel, President, INAE

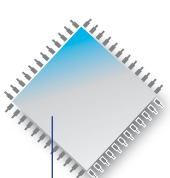
12:00—13:30:	Session I
13:30—14:30:	Lunch
14:30—16:00:	Session II
16:00—16:30:	Tea
16:30—18:00:	Session III
18:30—19:15:	Banquet Lecture by Prof. S.K. Brahmachari, DG, CSIR
19:15—21:00:	Dinner

01st November, 2009 (Sunday)

09:30—11:00:	Session IV
11:00—11:30:	Tea
11:30—13:00:	Session V
13:00—14:00:	Lunch

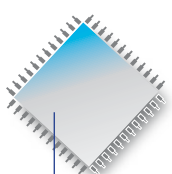
Session Themes:

- **Session I : Nuances and Challenges in Entire Design Cycle**
  Speakers: Aloknath De, Anurag Seth, Rajiv Jain
  Moderator: Jaswinder Ahuja
- **Session II : Killer Applications and Products in India Context**
  Speakers: Ganesh Guruswamy, P.Sridhar, Rajeev Shorey, Vivek Sharma
  Moderator: Subhash Bal
- **Session III : Competencies for World-Class Chip Design**
  Speakers: AB Bhattacharyya, P.P.Chakraborty, Jyotirmoy Daw
  Moderator: Prosit Mukherjee
- **Session IV : Leveraging on Design Ecosystem**
  Speakers: Jaswinder Ahuja, Rajat Gupta, Sunil Sherlekar
  Moderator: A.Vasudevan
- **Session V : Staircase to Powerhouse**
  Speakers: Chandrasekhar, Dinesh Sharma, Vivek Pawar, Ashok Madan
  Moderator: Aloknath De

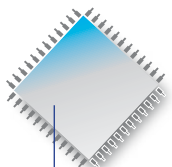


Workshop Participants

S. No.	Names	Organization
1	A Vasudevan	Vice President, VLSI, Wipro Technologies, Bangalore
2	AB Bhattacharyya	Emeritus Professor, Jaypee Institute of Information Technology, Noida.
3	Ajay Agarwal	President, Semitech Solutions Pvt. Ltd.
4	Aloknath De	Managing Director, ST-Ericsson India Pvt. Ltd.
5	Anala Prasad	TTM Pvt Ltd., Hyderabad
6	Anurag Seth	Managing Director (India Branch), Kawasaki Microelectronics
7	Ashok Madan	DGM (VLSI/Hardware Division), HCL Technologies Ltd., Noida
8	Chandrasekhar	Director, Central Electronics Engineering Research Inst. (CEERI), Pilani
9	Dinesh Sharma (in absentia)	Professor, Indian Institute of Technology, Powai, Mumbai
10	Ganesh Guruswamy	VP and Country Manager, Freescale Semiconductor India Pvt. Ltd., Noida
11	Jaijit Bhattacharya	Country Director, Govt. Strategy, Sun Microsystems, New Delhi
12	Jaswinder Ahuja	CVP and Managing Director, Cadence Design Systems India Pvt Ltd.
13	Jyotirmoy Daw	Managing Director, Mentor Graphics (India) Pvt. Ltd., Noida
14	KD Nayak	Director, Advanced Numerical Research & Analysis Group (ANURAG), Hyderabad
15	KM Bhardwaj	Group Director, Indian Satellite Centre (ISAC), Bangalore
16	Kulbhushan Misri	Design Manager, Freescale Semiconductor India Pvt. Ltd.
17	Manoj Dadhich	Design Manager, Freescale Semiconductor India Pvt. Ltd.
18	Mithilesh Jha	CEO, Masamb Electronics Systems Pvt. Ltd., Noida
19	MJ Zarabi	Vice-President, INAE
20	Poornima Shenoy	President, India Semiconductor Association, Bangalore
21	PP Chakrabarti	Professor & Dean (Sponsored Research & Industrial Consultancy), Indian Institute of Technology, Kharagpur
22	Pradeep Kumar	VP, STMicroelectronics Pvt Ltd, Grater Noida
23	Prosit Mukherjee	Vice-President, Transwitch India Pvt. Ltd., New Delhi
24	Rahul Hakhoo	Design Manager, STMicroelectronics Pvt Ltd, Grater Noida
25	Rajat Gupta	GM – India Operations, Beceem Communications Pvt. Ltd., Bangalore
26	Rajeev Shorey	President, NIIT University
27	Rajeev Srivastava	Design Manager, STMicroelectronics Pvt Ltd, Grater Noida
28	Rajeev Tiwari	Business Development Manager, Masamb Electronics Systems Pvt. Ltd.
29	Rajiv Jain	Managing Director , Infineon Technologies India Pvt. Ltd., Bangalore
30	Rajiv Kumar	Design Manager, ST-Ericsson India Pvt. Ltd



S. No.	Names	Organization
31	GV Ramaraju	Senior Director, Department of Information Technology, New Delhi
32	Reapan Tikoo	CEO, Powai Labs, Mumbai
33	RS Baoni	MD, Bisquare Systems Pvt Ltd., Noida
34	Sanjiv Narayan	VP & MD, Calypto Design Systems India Pvt Ltd., Noida
35	Satya Gupta	Consultant, Bangalore
36	SD Sherlekar	Founder & Head of Research, Computational Research Labs. Ltd. & Chief Scientist, Tata Consultancy Services Ltd., Bangalore
37	SK Brahmachari	DG, CSIR, New Delhi
38	Sridhar P	VP, Sasken Communication Technologies Ltd., Bangalore
39	Subhash Bal	Synopsys (India) Private Limited, Bangalore
40	Subind Kumar	Design Manager, Freescale Semiconductor India Pvt. Ltd.
41	Sunil Nanda	Consultant, NVIDIA Corp., Bangalore
42	Varambally Rajamohan	Director - TR&D India, STMicroelectronics Pvt. Ltd., Greater Noida
43	Vivek Pawar	CEO, Sankalp Semiconductor
44	Vivek Sharma	Head – India Operation, STMicroelectronics Pvt. Ltd., Greater Noida
45	VP Sandlas	Director General, Amity Institute of Space Science & Technology, Amity University, Noida



1. Background

1.1 India's Potential for Semiconductor Design

Semiconductor industry is becoming a major contributor to the GDP of most advanced countries. It is estimated that for every person on this planet, microelectronics industry manufactures presently about one billion transistors a year signifying the impact of semiconductor technology on human civilization. For last four decades, the average compound growth of semiconductor industry has been around fifteen percent. The microelectronics business is of the order of USD 290 billion and it virtually controls an electronics goods market of about USD 1.3 trillion.

India, with its sustained economic growth amongst Asian countries, is set to redefine the electronics landscape of the world. This is by virtue of its talent pool, internal market demand and growing status as nuclear/space power. It has been a chosen destination, for more than two decades, for multinational companies (MNCs) to carry out offshore semiconductor design-related business due to availability of English-speaking technical manpower in a cost-effective way. The expanding global fabless business model has triggered local enterprises and entrepreneurs to undertake VLSI design service-related operations, thereby creating strong competence base on the usage of EDA tools, design of Systems-on-Chip (SoC) and development of embedded system.

The backdrop of India's growing strength and stature in IT industry has provided an implicit and additional impetus to the evolution of VLSI design capability. The dramatic growth in number of technical institutions providing education in electronics, communication, information technology and computer sciences has been a positive development for knowledge-based VLSI design and embedded software industry. The proactive measures taken by the Government of India through establishment of National Knowledge Commission (NKC), and recent drive by Ministry of Human Resource Development (MHRD) to expand the base of IITs and NITs wider across the country; and creating a National Commission of Higher Education and Research (NCHER) is a clear message that India is destined to be a global technological power. Also, specific to semiconductor design, there have been special manpower development and research programs for VLSI in general and specialized topics like MEMS. Strategic projects such as indigenous microprocessor development for communication, defense, security and space exploration needs are also being envisaged.

The VLSI design and embedded software output from India is estimated to account for revenue generation of about 14 billion USD and creation of about 2,85,000 jobs in 2010. The figures estimated for 2015 are 40 billion USD for revenue and 7,80,000

direct jobs. An analysis of the technology adaptation, revenue generation and employment status reveals the following:

- *Though majority of offshore operations of MNC's are service-oriented, utilizing cost-effective Indian technical workforce, the operations have been responsible for design technology migration to India. This has created a strong semiconductor design competence, albeit not necessarily in the entire value chain in a balanced manner.*

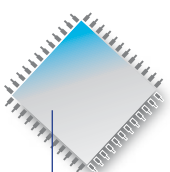
- *Currently, there are a few non-captive Indian industries incorporating the service oriented business successfully, especially in the embedded technology sector. These companies have garnered significant experience to participate actively with the clients to provide very cost-effective solutions and thereby add greater value for their clients.*

- *The future growth dynamics, however, seems to be dependent exclusively on external market forces due to which India is not able to harness the immense potential that semiconductor technology is capable of offering. It has not been able to position amongst nations which determine the silicon territory of the world. The silicon power of the world (S-7) is nestled with USA, Europe, Japan, China, Canada, Taiwan and Korea.*

- *There is strong indication that growth dynamics in silicon business strongly favors a shift of centre of gravity to Asia where India has a distinct advantage, provided it has a national perspective to seize such an opportunity. This is to be done with the development of competence in selected core sectors and setting up of a national apex organization involving key stakeholders to develop and implement a national roadmap for semiconductor technology on the lines that have been adopted by S-7 countries. Indian goal should be to develop technical competence and critical business to be a strong silicon power and position herself among the powerful nations and enlarging silicon conclave to S-8.*

1.2 The Workshop

In keeping with this realization, Indian National Academy of Engineering (INAE), in association with India Semiconductor Association (ISA) and supported by Department of Information Technology (DIT) and Office of the Principal Scientific Advisor to the Government of India, organized a workshop on the theme of 'Making India Powerhouse for Semiconductor Design' on 31 Oct—01 Nov., 2009. The workshop was attended by about fifty specialists and thought leaders in the field from industry, R&D and academia. They deliberated on issues related to India's capabilities---strengths and areas of improvement in the sphere of semiconductor design.



The discussion and deliberations were organized to address the following topics:

1. a) International microsystem technology highlighting IP and SoC design trends,

   b) The competence to develop end-to-end, full design for IP core and SoC,

   c) Adequacy of system knowledge for SoC and embedded design development.

2. a) Killer applications that can drive products in the market place,

   b) Opportunities for indigenous products in strategic, professional electronics, healthcare, consumer and energy sectors.

3. a) The level of skill and competence of the technical manpower in ASIC and SoC system design,

   b) Domain expertise in academic institutions,

   c) Industry-Academia collaboration in research and training,

   d) Product concepts/prototypes from university,

   e) Opportunities for innovation, intellectual property creation and required institutional, promotional and management structure.

4. a) The matured elements of the prevailing ecosystem,

   b) Barriers in leveraging the ecosystem,

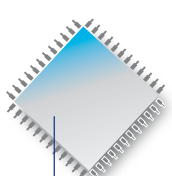
   c) Models for engaging design entities such as EDA, test, verification, embedded system with other relevant companies and enterprises.

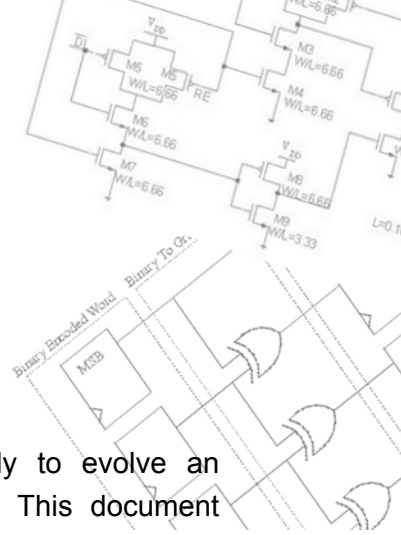
5. a) Prospects and roadblocks/analysis of constraints for India emerging as a VLSI/ SoC Embedded design powerhouse,

   b) Synergetic requirement for Fabless approach with outside foundry prototyping,

   c) Criticality of indigenous chip development for a secure defense, healthcare, communication and space program.

   d) Roadmapping/action plans in the short-term and in the long-term.



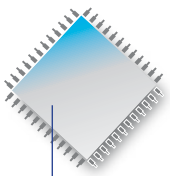


2. Nuances and Challenges in Entire Design Cycle

2.1 International Semiconductor Roadmap---Design

Semiconductor community has been working together globally to evolve an International Technology Roadmap for Semiconductors [ITRS]. This document outlines the trend of semiconductor technology evolution which serves as a guideline to anticipate challenges, priorities and opportunities. The roadmap serves as a reference which gets updated annually. The Table 1 is a sample (pertaining to high-performance MPU and ASIC product generation) extracted from the roadmap projection* of the process-driven design-specific scenario. The figures in the table are taken both as agenda and planning for design goals by international community for staying globally competitive.

The roadmap projection is broadly based on an optimal application of scaling laws to predict key performance parameters that characterize figure-of-merit of a digital building block. Supply voltage, gate capacitance including overlap, fringing components and the current drive, determine the intrinsic delay that can be judiciously estimated against a preset target of performance acceleration. For example, the drive current governed by threshold voltage, gate oxide, capacitance, mobility are required to improve by approximately 7-8% annually to ensure annual delay performance improvement of 17% over a period of eight years (2010-2018). Other features such as length (technology node) of microprocessor transistors is estimated to encounter a scaling of around 300%, supply voltage scaling by 30%, on-chip clock frequency to be pushed up by 350%, permissible maximum power dissipation by 15%, functional multiplication per chip by 600%. The migrating technology node, at which designs are to be implemented, is usually associated with new phenomena described by model parameters with which designers need to get continuously exposed#. As technology nodes are approaching physical limits, classical physics, is inadequate to describe device phenomena. Complex physical phenomena such as quantum effects, new scattering mechanism, mobility enhancement through strained silicon (s-Si), need to be included in the classical engineering design domain. Non-classical Silicon-on-Insulator (SoI) structures such as multi-gate/FinFET devices, metal gate devices, high-k dielectric gate etc. are expected to provide solutions to overcome physical limits of bulk CMOS and enable progress beyond Moore. Non-classical structures are likely to be routine building blocks for the designers. The breakthroughs at material/device area are to be integrated with multi-threshold, pass-transistor based circuit level approach to stretch the circuit performance limits related to complexity, power, frequency of operation etc.



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* *International Technology Roadmap for Semiconductors (ITRS) : 2009*

\# *A.B. Bhattacharyya, "Compact MOSFET Models for VLSI Design", John Wiley & Sons Pte Ltd. & IEEE, 2009*

TABLE 1: Table ORTC-2D High-Performance MPU and ASIC Product Generations and Chip Size Model																
Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Flash ½ Pitch (nm) (un-contacted Poly)(f)	38	32	28	25	23	20	18	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
DRAM ½ Pitch (nm) (contacted)	52	45	40	36	32	28	25	22.5	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	54	45	38	32	27	24	21	18.9	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5
MPU Printed Gate Length (GLpr) (nm) ††	47	41	35	31	28	25	22	19.8	17.7	15.7	14.0	12.5	11.1	9.9	8.8	7.9
MPU Physical Gate Length (GLph) (nm)	29	27	24	22	20	18	17	15.3	14.0	12.8	11.7	10.7	9.7	8.9	8.1	7.4
Logic (Low-vol. Microprocessor) High-performance ‡																
Generation at Introduction	p10h	p12h	p12h	p14h	p14h	p14h	p17h	p17h	p17h	p20h	p20h	p20h	p23h	p23h	p23h	p24h
Functions per chip at introduction (million transistors)	2,212	2,212	4,424	4,424	8,848	8,848	8,848	17,696	17,696	17,696	35,391	35,391	35,391	70,782	70,782	70,782
Chip size at introduction (mm^2)	520	368	520	413	328	520	413	328	520	413	328	520	413	328	520	413
*Generation at production ** *	p08h	p10h	p10h	p12h	p12h	p14h	p14h	p14h	p17h	p17h	p17h	p20h	p20h	p20h	p23h	p23h
Functions per chip at production (million transistors)	2,212	2,212	4,424	4,424	8,848	8,848	8,848	17,696	17,696	17,696	35,391	35,391	35,391	70,782	70,782	70,782
Chip size at production (mm^2) §§	260	184	260	184	260	206	164	260	206	164	260	206	164	260	206	164
OH % of Total Chip Area	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%	29.5%
Logic Core+SRAM (Without OH Average Density (Mt/cm2)	1,207	1,707	2,414	3,414	4,828	6,083	7,664	9,656	12,166	15,328	19,312	24,332	30,656	38,625	48,664	61,313
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	851	1,203	1,701	2,406	3,403	4,287	5,402	6,806	8,575	10,804	13,612	17,150	21,608	27,224	34,300	43,215
ASIC																
ASIC usable Mtransistors/cm^2 (auto layout)	851	1,203	1,701	2,406	3,403	4,287	5,402	6,806	8,575	10,804	13,612	17,150	21,608	27,224	34,300	43,215
ASIC max chip size at production (mm^2) (maximum lithographic field size)	858	858	858	858	858	858	858	858	858	858	858	858	858	858	858	858
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	7,299	10,323	14,599	20,646	29,198	36,787	46,348	58,395	73,573	92,697	116,790	147,147	185,393	233,581	294,293	370,786

VLSI manufacturing can now easily put hundreds of millions of gates or a couple of billion transistors on a single die at a reasonable cost. These manufacturing advances have enabled designers to create System-on-Chip (SoC) that includes most chips/components necessary for system. SoC design teams often make use of Intellectual Property (IP) blocks in order to improve their productivity. These IP's are pre-designed components that can be used in a larger design. It is projected* that SoCs of the complexity of 40 billion transistors will be designed in 2018.

Embedded system design is an outgrowth of cross fertilization of VLSI technology, communication system and computational techniques. It opens up numerous application domains thereby expanding the scope of VLSI design activity. The application domain drives the system architecture, platform architecture, followed by hardware/software implementation involving semiconductor design and prototyping. Embedded system brings about a radically new perspective in VLSI design business where conventional business model may provide space and opportunity for many new players in India.

In overall system design, some of the key engineering trends that are emerging: (a) Programmability in design, (b) Design at an abstract level, (c) System design verification/validation and so on.

Once used primarily as "glue logic", FPGAs today are key system-level components packed with features such as on-chip memory, clock management capability and programmable support for high performance I/O signaling standards. FPGAs allow equipment makers to significantly reduce their time to market. Further, because they are manufactured on the most advanced semiconductor process technologies available, FPGAs offer levels of design flexibility, performance and logic density that make them a viable and cost effective alternative to traditional fixed-logic ASICs. More important, FPGAs can be reprogrammed even after an end system has been deployed at a customer's site. As a result, FPGA technology is opening up a new area of equipment design that allows for hardware upgrades over a network. This promises to reduce equipment maintenance costs, extend the life cycle of products and create new sources of revenue for manufacturers by allowing them to add new features and capabilities remotely to installed products#.

Day-by-day, design is getting abstracted and defined at a higher level using system-level design. Electronic system-level (ESL) design is a set of methodologies that enables SoC engineers to efficiently develop, optimize and verify complex system architectures and embedded software. ESL design also provides the foundation for the verification of downstream register-transfer level (RTL) implementation. IC vendors have adopted ESL design to develop software-rich, multiprocessor devices that deliver the advanced functionality and high performance essential in next-generation devices$.

**Wally Rhines, "How to Design a 40-billion Transistor SoC", EDN, April 2010*

#*William S. Carter, "The Dramatic Changes in FPGA Technology", TechOnline Course.*

$*Seyul Choe, "ESL Enables Software-driven SoCs", EMS EDA 2005.*

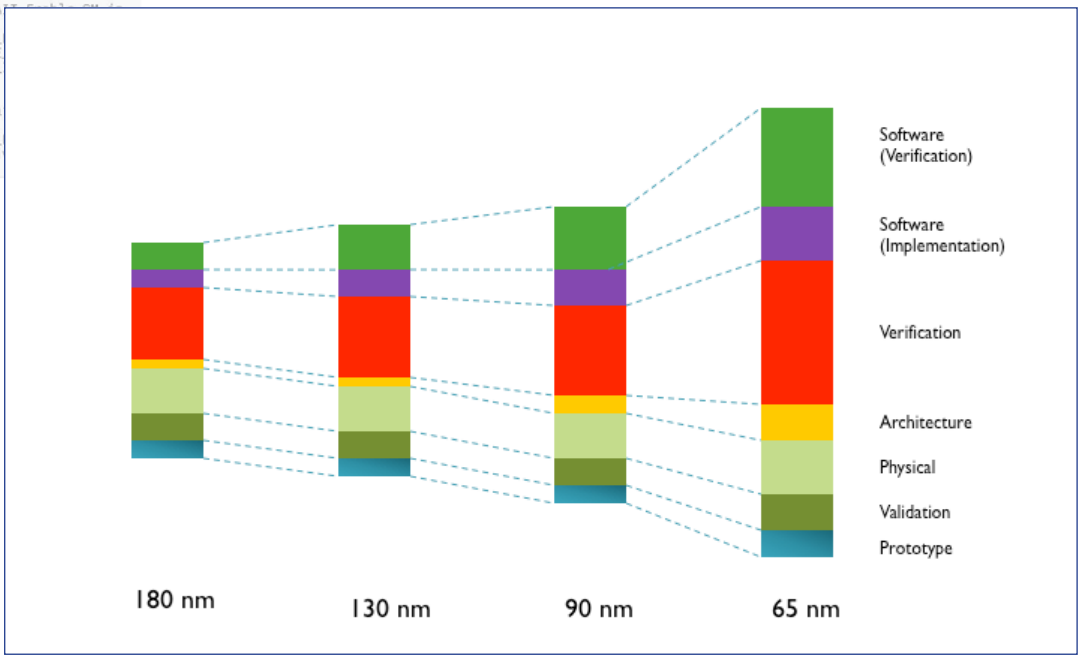
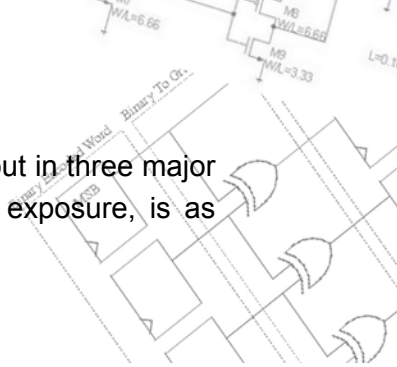


Figure 1: Verification challenge with increasing design complexity

Dunn's law proposes that for an embedded system verification/validation, methodology has to improve by a factor of four every 18 months which compared to Moore's law of growth complexity by a factor of two for every 18 months, indicates a threatening gap developing in the verification domain. Validation/verification methodology of embedded system at software level is based on data structure, algorithm etc. which have not progressed as fast as semiconductor technology. This is an area that represents a barrier and opportunity. Given the hundreds of millions of transistors on a chip, capturing the complexity of an SoC into an executable verification environment and then performing formal verification at every step of the design flow can become a mammoth task. Modeling performance around transactions and bus functional models facilitates in creating reusable verification code. Verification at multiple levels is becoming a trend. Figure 1 shows how verification activities have been evolving over technology node progress.

2.2 Salient Observations

- **Transformation in Design:** In order to deal with increasing complexity and shortened product life cycles in a competitive market, design cycle time needs to be reduced. New design methodologies for faster implementation, verification, and testing are being developed. Refinement of SoC design strategies for architecture, front-end and back-end implementation, DFT, validation, and overall integration is also taking place continually. Significant changes are thus anticipated in the next few years. Countries which are fast to pick up the changes stand to benefit in market place. We need to dynamically adapt ourselves to this "transformation in design".



- **Phases of Design:** Design activities are generally carried out in three major phases in which India's corresponding status, in terms of exposure, is as follows:
    - Specifications & Architecture – Low Exposure
    - Design – Reasonably Good Exposure
    - Testing – Medium Exposure

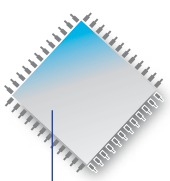
  We need to bridge the gap in our ability of architecturing and testing to be able to do the entire system design ourselves.

  In respect of specification and architecture, mindset of engineers needs to be changed as this phase demands being able to deal with fuzzy situation and ill-defined problems. In fact, this phase requires strength in conceptualization and requirement-assimilation/analysis. We need to seek/create opportunities for complete chip design. Based on the specification of an intended design, engineers implement timing-critical components like CPUs or function-critical analog components as hard macros. On the other hand, functions without any critical-timing requirements are implemented as soft macros. As more local markets get developed, new chip and customization requirements emanate. Gap in the architectural phase of the work as well as the need for active participation in standards committees has to be addressed to be able to gain design autonomy.

- **Hardware and Software Co-design/Partitioning:** With co-design of hardware and software becoming a norm, partitioning so as to define which algorithms are to be run in hardware and what should be implemented in software is a critical skill set that we need to cultivate. Our software strength could be used extensively to model chips and validate execution of algorithm even though it is run eventually in hardware. To emphasize, India's established position and capability in software domain could be leveraged to great advantage.

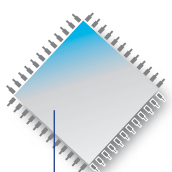
- **Domain Specific Design Strength:** India doesn't have very many players having domain-specific design strength. Expertise is indeed lacking in many areas (e.g., analog and mixed signal, RF design etc.) which are critical for completely independent product design. Tomorrow's market drivers are: analog components including analog IPs and digital entities having Near Field Communication (NFC) provision. These as well as expertise in system-level specification and design are thinly available.

- **IP Design vs SoC Design:** IP Design requires depth/domain knowledge whereas SoC design requires breadth/integration knowledge. Even while our large manpower resource base continues to be involved in SoC design, we need to consciously work towards building up of a portfolio of world-class IPs which might of necessity even involve Venture Capital (VC) funding. While this could



be expected to happen with growth in knowledge base and entrepreneurship, there is an urgent need to adopt proactive approach to promote/encourage building of expertise in specific/niche design technologies and thereby create specialized professionals/national experts who would in turn play a critical role in furthering business in those areas.

Building critical IPs at national level (e.g., India processor, configurable DSPs etc.) driven by national pride, security or market potential is considered essential. Conducting national level design contest(s) with particular emphasis on innovative IPs, SoC architectures and products could go a long way in encouraging this culture.



3. Driver Applications and Products

3.1 Product Trend

Globally, the size of electronics industry is approximately two-and-half times that of oil/petroleum industry and about the same size as that of the electricity market. Electronics and semiconductor industry, which is fast growing compared to chemical, automobile, oil or textile industries, has been showing a strong correlation with the GDP of a nation over the years. Figure 2 below shows region-wise growth of the worldwide electronics industry.

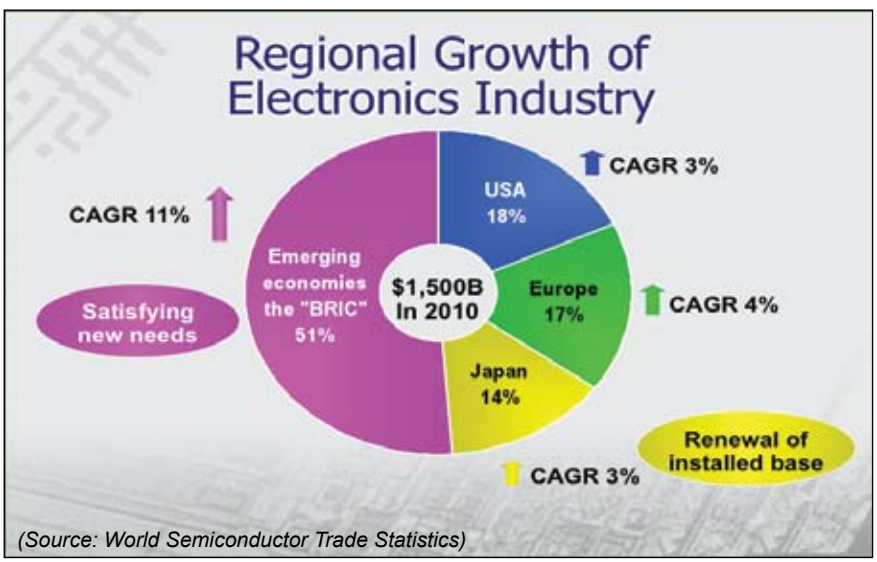


Figure 2: Regional growth of electronics industry

Worldwide, technology trends are bringing smarter, slimmer, converging-solution-based products across all segments of industry and infrastructure, viz., entertainment, personal multimedia, communication infrastructure, computer peripherals, health, energy and transportation applications. Certain miniature health devices based on low-power solutions are good examples of convergence of consumer products with healthcare products. Technology is facilitating ICT-enabled services in e-learning and e-governance in a significant way. Cell phones are becoming smarter and richer in terms of applications at great pace. SoC-based designs simplify the end-system design as it integrates several previously designed distinct functional blocks on a single chip. Today's SoCs are making the vision of an open architecture for mobile multimedia a reality and driving the design of ultra-light, pocket-sized, multimedia-enabled mobile phones. In fact a mobile phone is no longer just a portable alternative to fixed line phone but has already become the multi-tasking work horse enabling the user to access emails, surf the net, get directions, play music and videos and also shop.

Semiconductor content has been growing as intelligence is embedded in modern

devices and appliances. This is evident from the Figure 3 below which gives the increasing semiconductor pervasion in electronics equipments over the years. It is interesting to note that in automotive, semiconductor content has grown five-fold in the last thirty years.

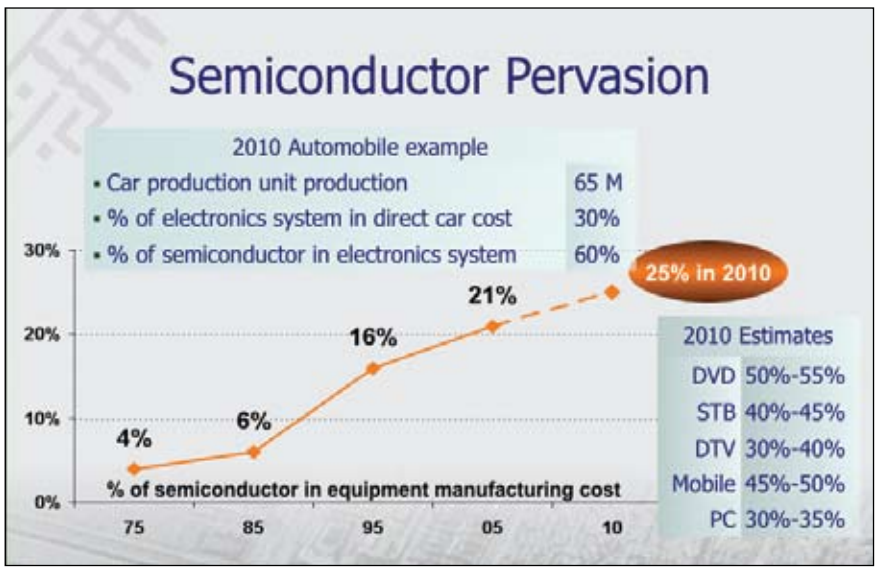


Figure 3: Semiconductor pervasion

3.2 Salient Observations:

- **World of Imbalances:** Empirically, it is observed that the electronics goods consumption and semiconductor market size are strongly correlated to gross domestic product (GDP) of any developed/developing country. India with 17% of world population accounts for 2% of GDP whereas USA with 4.5% of world population accounts for 25% of GDP. Such economic imbalances (see Figure 4) can be seen to present a great untapped market potential. India's

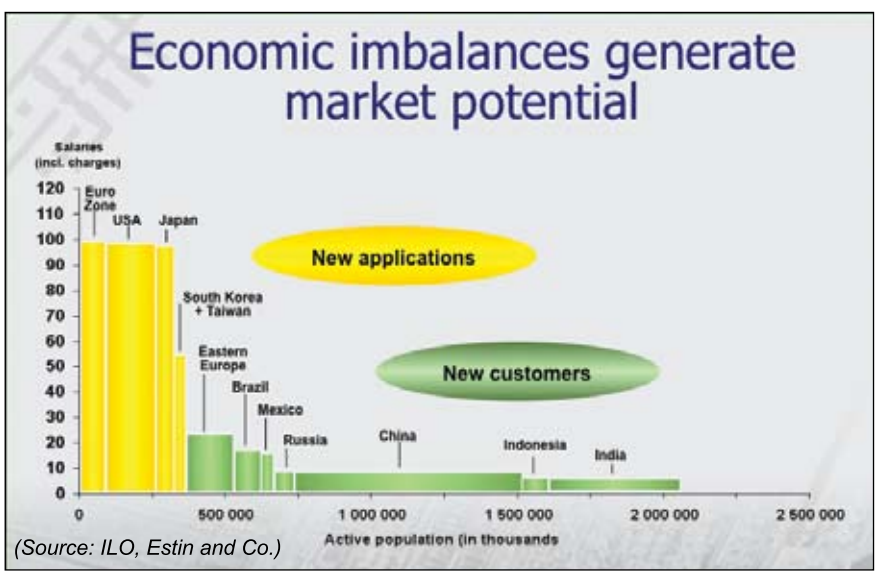


Figure 4: Economic imbalances generate market potential

sustained 8-9% growth in the years to come would, besides improving the economic well-being of the country, help bring a certain balance in the world economic order. Given its pervasiveness in all sectors of industrial and infrastructure development activity, semiconductor will undoubtedly act as a major enabler in this regard.

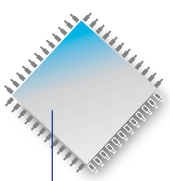
- **Inflection Points:** In the nineties, India emerged as a cost-effective destination for seeking IT and IT-enabled software services which after some years was followed by acquiring a similar position in the area of VLSI design. Since 2007, however, cost-effectiveness advantage seems to be fading; the need now is to focus more on market development---strengthening and segmenting products across markets. With all the experience designers have garnered over the years, it has now become important to go up the value chain from semiconductor design to system level product conceptualization and development.

- **Market Perspective:** The rapid industrialization of India, coupled with growing middle-class population, points to the emergence of an indigenous market with products defined specifically for its development dynamics. Like nuclear energy and space programs, India must envision to get integrated with global silicon-powers adapting their growth model suitably tailored to its own conditions. Due to synergetic approach, increasing success of fabless operational model, employment and intellectual property (IP) generation potential, higher scope of entrepreneurship, relatively low capital requirement and acquired competence base, the time is ripe to strategize and build an India vision for becoming Semiconductor Design Powerhouse.

  It is imperative to understand markets as such and also learn how to create markets based on soft or hard needs. We need to build our sensitivity to product features offered, price-performance point, product mindset vis-à-vis service orientation. For this purpose, interested semiconductor design companies have to nurture an application lab and also work with Original Design Manufacturers (ODMs). The much needed cost reduction/optimization for Indian market will also lead to 'reverse innovation' and create significant market in developed countries once the product is tested in local markets.

- **India-Specific Products:** While there is a boom in a number of sectors, India's growing needs for products is in power, healthcare, education and communication industry and infrastructure sectors.

  Power requirement which is expected to double to about 400 GW by 2020 will involve an investment of about USD 600 billion. The need for reducing T&D power losses which presently stands at about 40%, that for improving energy efficiency in our routine usage of power (scope of reduction believed to be to the extent of 50%) as well as for meeting the needs of power management in the renewable energy sector, presents great opportunity for designing



India-specific products. Automatic Meter Reading (AMR) devices, feature Electronic Energy Meters (EEM) as well as prepaid EEMs, High efficiency and high reliability Solar Inverters are some of the examples for this sector.

Role of electronics in general and semiconductor devices in particular in healthcare industry is to be recognized with the industry expected to grow to USD 40 billion by 2012 and USD 280 billion by 2022. Low cost consumer and portable (using low power) devices such as handheld ECG Monitor, non-invasive Glucometer, Pulse Oxymeter, imaging devices are examples of products insofar as medical diagnostics aspect of the healthcare industry is concerned. Embedded internet devices, wearable computers and newer diagnostic devices (such as saliva and breath analyzers) are tomorrow's market drivers from semiconductor design point of view. One could even think of an innovative H-pod product for India market. It may be emphasized that demographic profile of our country as well as the need for low-power, low-cost solutions requires to be taken into account while designing such devices. Intelligent hospitals, mobile hospitals, tele-medicine and remote surveillance using wireless technology are other aspects of this industry that together with the medical diagnostic devices represent enormity of opportunity that exists in the sector.

In our endeavor to provide education to all, low-cost laptops alongwith internet connectivity, e-reader/smart books are among many products/gadgets that make a case for innovative design. There is scope for encouraging comprehensive usage of IT/semiconductor technology in the e-governance and financial inclusion schemes of the Government.

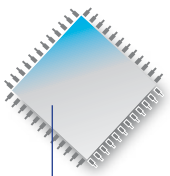
Product positioning is part of product development. It is clear that language-specific development (with ethnic diversity in India) and ability to define new standards for next-generation products (e.g., Chinese standards of TD-SCDMA) will become important drivers for product development. Innovative applications and products would afford introduction of new services and productivity enhancement. Development of a family of products through programmable software that would also facilitate personalization could be a thrust area.

There are a few other products that need to be considered for meeting our market needs and at the same time for bolstering semiconductor design and product engineering capability of the country. These products could also leverage the strength of industry and academia using cutting-edge technology. An example of such a product that merits serious consideration is the CMOS-MEMS based uncooled Focal Plane Array (uFPA) for infra-red thermal imaging for defence as well commercial applications. Because they do not require the use of a cryogenic cooling unit, infrared cameras that use uncooled detectors enjoy substantial advantages in maintainability as well as a significant reduction in

size, complexity and cost.

- **India Processor:** Despite having many sophisticated processors and microcontroller cores in the market place, it is important for India to have its own processor for strategic reasons. In China, recently a netbook computer has been launched at a price tag of $99 using an indigenous processor* An indigenous processor, serving most of our strategic needs, can help the country to be worry-free from spyware/malware and help launch new products at affordable price promoting social inclusivity. While building on the already available expertise in DRDO and elsewhere in the country, India Processor should be developed as a core with needed tools to serve as a platform around which SoCs/applications, particularly of strategic importance (such as routers for secure communication) can be developed thereby ensuring technology sovereignity.

- **Innovation and Building of IPR Portfolio:** It is believed that India is not socially conducive for innovations that would require significant investment in the hope of major economic gains. With stigma associated with failure, many people would rather not try and make any serious attempts at innovation. This risk-aversion mindset requires to be changed, particularly among hi-tech engineering professionals. In their endeavour to build innovative products, Indian professionals and companies should strive to file patents both in India and abroad. Building of patent portfolio/IPR assets becomes important for companies irrespective of strategies to deploy them in product development or trade with other companies for mutual benefit. At country-level, we should partner with premier institutions of other countries (like IMEC of Belgium) and find practical solutions for cross-patenting and patent leveraging.



* *Peter Clark, "Chinese Processor Drives $99 Netbook", EETimes, Dec.2009.*

4. Competencies for World-Class Chip Design

4.1 Global Competencies for Semiconductor Design

VLSI design, being very complex and knowledge-based, requires an environment for high-level of innovation pursuit, supported by industry-level infrastructure. The fact that industry-standard infrastructure can not be provided to all institutes, a model is now in place internationally such that academic and research institutes can access industry-standard manufacturing facilities. Therefore, it is appropriate to have a look at the model adopted by S-7 silicon nations. This will help us in suggesting an approach for microsystem competence building in universities and technical institutes comparable to countries leading silicon revolution. It is observed that each of the countries belonging to S-7 group have a nodal coordinating organization in one form or the other, as listed in the Table 2, to steer the national agenda on semiconductor chip design with emphasis on competence building.

TABLE 2: Microsystem Competency Building Initiatives- S-7 Countries

Country	Organization	Year of Formation
Canada	Canadian Microelectronics Corporation (CMC)	1984
China	China Integrated Circuit Design	2000
Europe	Euro-practice/Circuit Multi-Chip (CMP),	1981(CMP)
Japan	VLSI Design and Education Centre (VDEC)	1996
Korea	Integrated Design Education Centre (IDEC)	1995
Taiwan	Chip Implementation Centre (CIC)	1992
USA	MOS Implementation Service (MOSIS)	1981

VLSI design activity can be broadly classified into two categories: Circuit–on-Silicon (CoS) and Systems-on-Chip (SoC). The CoS is pertaining to design prototyping on silicon through a foundry service, internal or external. On the other hand, SoC (or even System-in-Package) is related to product or system development and is in most cases centered around processors with software co-design.

SoC design* has been a growing area where the pedagogical planning has to be linked to system development and application. There is need to proliferate multiprocessor based system-on-chip design through large scale distribution of

Aloknath De, "SoC Design in India", EDN Asia, Dec 2005

domain-specific (e.g., communication) system level platform amongst educational institutes to generate system-centric awareness. System-level integration also requires support to integrate array of diverse technologies in a single package which requires access to packaging, bonding, bread-boarding, testing etc. Access to such diverse and specialized facilities within a short time-frame is an important factor for proliferation of the SoC design culture. Functional verification for SoC designs has assumed great importance which indeed accounts for nearly 50% of the design effort/manpower resources comprising the design team. Verification, particularly now required at different levels of design process, has thrown many challenges and opened opportunities in its wake. It has required emphasis on learning new languages, methodologies and tools.

It turns out that in S-7 countries, generally design prototyping on silicon has been integrated in the UG and PG curriculum in such a way that the students are in a position to complete full design cycle including testing and packaging within the project implementation schedule. Indian VLSI design education appears overly theoretical in comparison. It is time that the postgraduate project planning is recast. Most of Indian design prototyping seems to have been outcome of Ph.D. research or Masters program spread over more than one batch. Therefore, it is important to orient these programs to provide design skill base coupled with silicon design experience as well as introduce practical design concepts early on through undergraduate programs.

4.2 Salient Observations

- **Special Manpower Development Program (SMDP):** There have been several initiatives from Government of India to support human resource development in the area of VLSI Design. The most significant has been Special Manpower Development Program (SMDP)-Phase II, through which about 30 Design Centers have been created with Five IITs, CEERI and IISc acting as nodal agencies. The program has made industry-standard software and EDA tools available to the centers. The program also provides an interface with external foundry for siliconizing designs selectively for cases which meet required benchmark set by project-steering panel. It appears that in spite of forward-looking initiative of the Government, there are gaps and logistic problems that need to be addressed to make the initiative attain the intended objective.
- **Nationally Coordinated Specialized Programs:** The other support to educational institutes comes from programs like NPMASS. This Union Cabinet approved program, piloted by the scientific departments with the responsibility of administering the same by Aeronautical Development Authority of DRDO, was meant to launch a nationally coordinated activity on development of smart materials and sensors. The program has created 30 design centers across the country to be coordinated by six nodal level-one institutes around IITs and IISc. Primarily dedicated for MEMS design and development, the

program envisages foundry support for appropriate cases. The program has arrangement for training on software by the suppliers of tools. CEERI-Pilani is identified for training in MEMS processing and SCL-Mohali as well as SITAR-Bangalore are identified for production and prototyping at the national level.

- **VLSI M.Tech and Capsule Programs:** The SMDP program has been able to create awareness in technical institutes on the importance of VLSI design in electronics engineering curricula due to which even undergraduate courses in large number of institutes now teach basic CMOS design and VHDL-based digital design. Many centers have started running M.Tech. program in VLSI Design and/or embedded system successfully. The above programs, coupled with large number of post-school capsule programs of six months to one year duration, have been able to meet the manpower need of VLSI industries for the current service-level operation of VLSI Design prevalent in India.

- **Near Absence of Design Prototyping on Silicon by Indian Universities:** Statistics (see Table 3) reflect that universities in S-7 countries, Canada, China, Europe, Japan, Korea, Taiwan and USA, have respectively prototyped design on silicon using foundry facilities in numbers as large as 378, 400, 433, 170, 900, and 1400 on the average annually. The study also shows that the universities in these countries, on an average, are showing an increase of about 20% in number of chips fabricated annually. In addition, the number of universities joining the club using foundries for VLSI design education is also increasing by about 10%. In contrast, design prototyping from Indian Universities is of the order of a few tens annually. The performance of Indian universities turns out to be alarmingly poor regarding silicon experience of design.

TABLE 3: Benchmark: S-7 University Design Competency

Benchmark: S7 Univ. Design Competency

Country	Period	Design Prototyped	Tech. Node	No. of Univ.
CANADA	2007	378	65 nm	3000 (s)
CHINA[1]	2007	48	90 nm	20 (u)
EUROPE	1982–2007	3,654	95 nm	195 (u)
JAPAN	2007	433	0.18 µm	55 (u)
KOREA	1995–2008	1,814	0.18 µm	60 (u), 3700 (s)
TAIWAN	1992–2008	9,044	90 nm	80 (u)
USA	1981–2008	12,500	65 nm	50,000 (u)
INDIA	2002–2009[2]	50-60	0.18 µm	5 (u)

1 CHINA-STM Tie-up for 65 nm technology for university chip design
2 extrapolated

The yawning gap between our universities and those of S-7 countries in the area of design prototyping on silicon is also reflected in our very poor

record of publication of design related research in representative international professional journals such as IEEE Journal of Solid State Circuits, IEEE Transactions on Computer Aided Design etc.

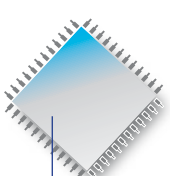
EDA tools constitute an indispensable component in Semiconductor/VLSI design activity. Universities in general have spearheaded development of EDA tools in nations leading microelectronics revolution. Inspite of India having positioned itself relatively strongly in the area of software including embedded systems software, this software base has not translated in seizing the opportunity in contributing to the development of EDA tools. Lack of rigorous research in modeling and much needed interaction with software professionals towards developing a specific tool may in fact be the root cause.

Another aspect implicitly related to chip design is the Intellectual Property management structure within the academic institutes. While some awareness seems to be in place regarding patents, it is realized that lot needs to be done in fostering an environment for creating and preserving archives for the intellectual property that academic institutes are destined to create.

- **Lack of Design-on-Silicon/IP Design Competency in India:** The statistics for Design-on-Silicon/IP Design could well be used as a metric of design competency. The reason for lack of this competency in India can be attributed to:
  - Lack of faculty competence in design-on-silicon.
  - Lack of industry-academia interaction on silicon design which could reduce the gap through participation of industry-based experts.
  - Inadequate coordination mechanism with foundry.
  - Poor curriculum planning to make full design flow materialized in VLSI design courses.
  - Lack of access to testing, failure analysis tools and bread-boarding facilities coming in the way of reaching end goals in design.
  - Absence of domain expertise to undertake purposeful designs with innovation and intellectual property attributes.
  - Lack of understanding of application and specifications from users, making design exercise divorced from real-life problems relevant to industry and society.
  - Lack of accountability to use available resources optimally.
- **Need to Emulate S-7 Countries' Silicon Initiatives in Education:** Looking at S-7 countries, it is observed that initiative in education has been given a very high priority recognizing that the silicon industry is knowledge-driven. If India is to aspire to be part of the silicon conclave thereby extending it to a consortium

of S-8, we need to capture the initiatives undertaken by S-7 countries and suitably adapt to Indian strategy on a priority basis. Significant initiatives required to be taken on the pattern of S-7 countries are listed below:

- Design on silicon to be emphasized; focus should be on breakthrough design.
- Need to have domain and IP expertise groups; encouraging products coming from academic institutions.
- Emphasis to be on basics and pedagogy; course contents to be put online and networked nationally.
- Access to fast prototyping/foundry facility to students as well as to regional/ national support facilities (to be created as required) for testing, failure analysis and bread-boarding.
- Multi-Project Wafer (MPW) runs allow sharing of cost amongst clients and thereby reducing the die cost within the reach of universities. In some countries, for class projects, the cost is entirely or partially subsidized by the government.
- Identification and periodic updation of a bank of projects, coordination and multi-institutional participation.
- Involvement beyond EECS and beyond IITs/IISc to widen the base from Tier-I institutions to Tier-II institutions; Tier-I institutes to mentor Tier-II institutes in the neighborhood.
- Industry as stakeholder: design implementation in academic institutes with project sponsorship from industry. Foster industry-academia interface through active involvement of industry personnel and support of specialized facilities/tools.
- Board of Studies of colleges/universities to have representation from industry to reflect the need of industries and job opportunities.
- Industry experts to be encouraged to participate in teaching and project implementation/evaluation.
- Provisioning for soft, hard and wet labs; and encouraging new age entrepreneurs.
- Development of skills pertaining to chip architecturing and specifying, where we seem to lack exposure, needs to be garnered.
- De-integration movement - a move towards pure analog and pure digital – that appears to be in the offing would require to be kept in view.
- Focus on setting up a Failure Analysis facility and introduction of topics covering defect density of fab and yield engineering as part of the curriculum.



5. Leveraging on Design Ecosystem

5.1 Ecosystem Elements

Various ecosystem elements are prevailing in the semiconductor industry---development ecosystem, manufacturing ecosystem, supply-and-demand side ecosystem, Business/Govt/Policy-related ecosystem. India can not skip manufacturing completely. The manufacturing ecosystem could be subdivided into (i) Fab-related ecosystem and (ii) System-related manufacturing that definitely needs to be developed and, in fact, to be considered as a pre-requisite for having semiconductor fabs in India. With Special Incentive Package Scheme (SIPS) policy of Govt. of India, fabs are starting for solar photovoltaic cells. This is a good start before we go for full-fledged semiconductor VLSI fabs in India. However, in this report, we concentrate on the ecosystem that enriches semiconductor design process. Focused actions on design related issues alone can pay rich dividends even after we have the highly capital-intensive manufacturing. System level and ODM companies are significantly less in India. Acceleration of electronic equipment design and manufacturing in India would promote direct chip consumption. Figure 5 shows constituents and example companies that are part of the design ecosystem.

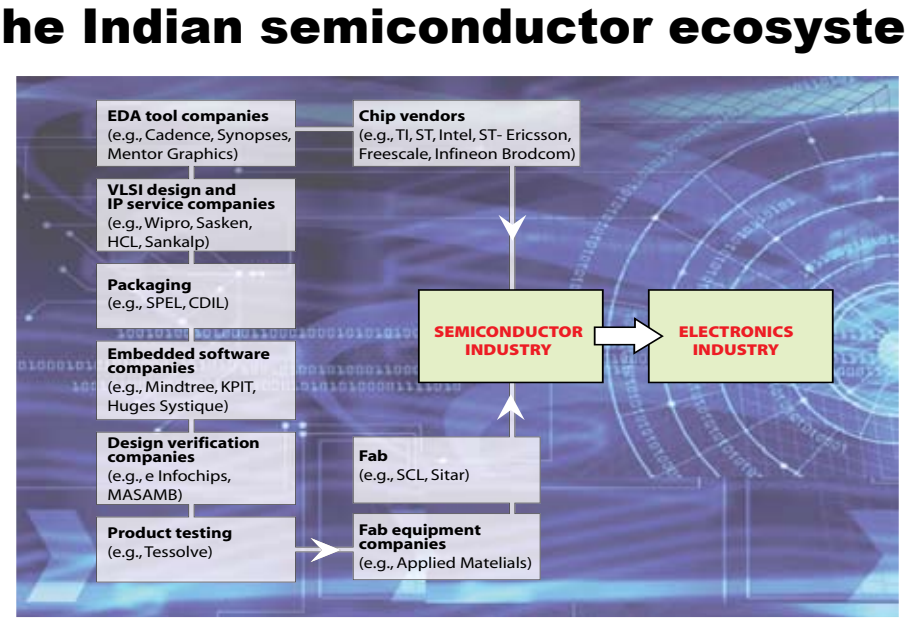


Figure 5: The Indian semiconductor ecosystem

5.2 Salient Observations

- **Design Ecosystem:** The major elements of design ecosystem, namely, domain, EDA software support and potential domestic demand do exist in the country. Yet, we have not so far been able to leverage this design ecosystem

well enough, perhaps due to (i) emphasis thus far on offering design services and not exploiting the potential Indian market, (ii) local industry operating in specific domains not showing enough enthusiasm or courage to do their system-level product design incorporating their own proprietary semiconductor design, (iii) lack of intense investment in R&D, particularly in industry and somewhat tight fisted approach of the Government in respect of liberal R&D support to the industry in the private sector including the much deserving start-up companies, (iv) absence of intense industry-academia interaction (where is our Boston?) and very importantly (v) *absence of national agenda* for this critical/strategic and economic activity.

- **Value Capture vs. Value Creation:** Apparently, design ecosystem in India is quite developed; yet we don't have effectively any Indian semiconductor companies. Almost all are MNCs having captive centers in India. Although 'value creation' is happening, we are not doing any 'value capture' for Indian products.

- **Products in India commensurate with Purchasing Power:** Changing Industry structure and growth patterns will drive the growth in future. Service model doesn't lead to ownership. Keeping in mind purchasing power of people in India, products need to be conceptualized particularly for bottom-of-the pyramid. Fundamentally sound products with less frills are the objectives. Indian market definitely plays proxy for other developing countries. But, also the base product with correct cost structure will serve as basis for more sophisticated products meant for upper population segments and developed countries. Price points will be set much more appropriately even for the higher segment products.

- **Innovative Start-up companies:** Start-up companies spur innovation and require to be nurtured. Financial institutions can play a crucial role by providing soft loans to entrepreneurs along with VC funding. Besides, DSIR and other agencies grants, in addition to soft loans, can help incubating new product ideas. Entry, exit rules as well as government shares, organizational control require definition. Legal and financial barriers could be addressed by learning from startups model in UK, Singapore. Successful models like Cambridge technology park need further exploration.

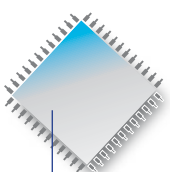
- **Quality Interaction among Stakeholders:** Leveraging the design ecosystem could lead to needed proliferation of fabless companies. This is particularly possible if Govt. comes up with Design Parks and provides necessary infrastructural support. EDA companies can also allow pay-per-user licensing to stimulate design activities. Decision making in most existing design companies in India being done overseas, a startup company capable of developing IPs and any glue tools finds it normally difficult to sell its ware to these design companies. More complete designs locally done will help strengthening the

ecosystem.

- **Product Testing and Failure Analysis Facility:** Even for the level of design knowhow that is available, one of the major deficiency stem out of inadequate testing, characterization and failure analysis facility. This deficiency will prove to be more inhibitive as we try to mature in our design capability. Need for regional/centralized test and failure analysis facility(ies) appears to be a crying need.

- **Need for a "slim" Fab:** The design ecosystem would undoubtedly be strengthened by the availability of prototype-cum-low volume manufacturing fab which at this juncture would only be possible through government support. This fab could be "slim", but continually upgraded in terms of technology capability. SCL-Mohali which is now under Dept. of Space and is understandably being upgraded from 800 nm to 180 nm could have possibly met this need. Many of the S-7 countries have one such fab of their own.

- **Environmental Considerations:** As part of the ecosystem, regulatory agencies need to address electronic-waste management and simultaneously measure SAR (Specific Absorption Rate) and waste materials' effect on human body. In the design stage, environmental considerations can be captured; but more serious monitoring will be needed when we start to manufacture products locally.



6. Staircase to Powerhouse

6.1 India among Engines of Global Growth

International studies indicate that, by virtue of human resource availability and growing middle-class populace, there will be plethora of product design and service opportunities in Asian countries. Will India be able to grab Asian opportunity to emerge as a global semiconductor design power? In fact, India was one of the first countries in Asia after Japan to start production of semiconductor devices. Initial head start has not helped us to gain our rightful place. It is imperative and indeed high time that we make a change from our earlier mindset of developing **'domestic competence'** to becoming a **'global player'**. We need to move from segmental design implementation to complete design including full-chip architecture. India is a good source on talent supply side, but currently is missing the market flavor and thereby specific requirements for innovative products. Indian market is destined to grow rapidly and we stand to be in an advantageous position in competition.

Needless to say that the new opportunity is also associated with the new challenges such as capability to handle increasing complexity of product that is heterogeneous and require multi-disciplinary approach, intelligent services and highly evolved project management structure. The following are some of the more specific challenges that the emerging design technology related scenario presents which call for enhancement of our competence/capability to do world-class chip designs to serve global market place as well as address our own evolving market:

- The activity of chip design now demands much larger gamut of expertise involving circuit design, analog-digital mixed signal, SoC and system-level simulation and verification.
- Data communication with multilayer architecture is the emerging business for semiconductor chip industry as multimedia and device-to-device communication are gaining momentum.
- Elaborate power management for connected network devices.
- Attainment of design productivity with increasing complexity.
- Cost of development.
- Emphasis on zero-defect design in order to ascertain product safety and also avoid any cost of recall/defect.
- The Integrated Device Manufacturers (IDMs) leaving space in favor of more and more fabless solution providers supplying intellectual property (IP) blocks, design, testing, packaging and board-building-up services. Such

a decentralized structure creates new sets of opportunity windows, which is of significant relevance to India where vertically integrated structure is conspicuously absent.

6.2 Recommendations

India has to climb up many steps to become 'Powerhouse for Semiconductor Design'. A consolidated view of these steps/recommendations, both in short and medium term, is presented in the following.

- Applying conscious and proactive effort to **change the broad character of the industry** from service-provisioning to product-orientation.
- **Quality manpower generation** on a wider scale of design technologies. Although SMDP program is an initiative in right direction, it can be tailored for more result-oriented design targets. With cloud computing and new licensing models for EDA, many users and institutes could be accommodated fueling growth. Furthermore, sponsorship of students at M.Tech. and Ph.D. levels from industries and user organizations would go a long way to develop high-end qualified manpower.
- **Recasting the post-graduate program** to ensure that full VLSI design flow can be implemented at least in graduate level projects. The projects may be formulated taking into consideration the needs of various sectors of Indian industries---defense, space, environment, energy, healthcare etc. Semiconductor design technology can play a pivotal role in addressing pressing national problems in these sectors. Project grants should be made jointly to university and Industry.
- Identifying **selected domains for expertise development** such as low power design, analog, RF and mixed signal design, System-on-Chip design; and forming country-wide study groups for drawing roadmaps for targeted expertise development in these areas.

  Building capability of developing compact device models for circuit design and simulation as well as EDA glue tools (and even complete tools) in certain niche areas is also required for an integrated design ambience.
- **Provisioning of end-to-end chip design-related services:** Wide-scale access to fab, chip testing facility and failure analysis (FA) tool are required for more design-on-silicon activities vis-à-vis present state where very few designs go from academia and R&D for chip prototyping. The number of designs going on silicon could be targeted to at least 100 per year in the short term.
- **Design of affordable products** for bottom-of-pyramid population through

disruptive approaches in terms of specifications, cost goal or both. This will lead to 'reverse innovation' that will also help bringing down cost of high-end products.

- While building on the already available expertise in DRDO and elsewhere in the country, **India Processor** should be developed as a core with needed tools to serve as a platform around which SoCs/applications, particularly of strategic importance (such as routers for secure communication) can be developed.

  Another product that merits serious consideration is the CMOS-MEMS based uncooled Focal Plane Array (uFPA) for infra-red thermal imaging for defence as well commercial applications. Because they do not require the use of a cryogenic cooling unit, infrared cameras that use uncooled detectors enjoy substantial advantages in maintainability as well as a significant reduction in size, complexity and cost.

- **Proliferation of fabless companies** with innovation potential for well-defined meaningful projects and products through liberal financial support by Government and other agencies.

  Start-up companies spur innovation and require to be particularly encouraged/ nurtured. Financial institutions can play a crucial role by providing soft loans to entrepreneurs along with VC funding. Besides, DSIR and other government agencies can provide grants in addition to soft loans to help incubate new product ideas. Entry, exit rules as well as government shares, organizational control require definition. Legal and financial barriers could be addressed by learning from startup models in UK, Singapore. Successful models like Cambridge technology park needs further exploration.

- There is not enough happening in respect of **Private-Public Partnership (PPP).** Govt. organizations like CSIR, ISRO, DRDO, DAE need to open up and proactively solicit involvement of private industries. Also, relevant public sector companies like BEL, ECIL can bring in the elements of strategic partnership and seek to add value in their collaborative arrangements with foreign companies as well as involve local private industries in their downstream activities. Thus, PPP model has to be made more effective, particularly for socially meaningful products.

- **Upgrading facilities in Tier-II cities** and promoting incubation/innovation center clusters involving the universities and local companies/entrepreneurs.

- Deliberating on semiconductor strategy to be linked to the need and viability of a national silicon foundry. It has almost been a unanimous opinion of the workshop that in the short term design competency can be carried out streamlining the coordination with an external foundry but in the long term there is no alternative to having at least a research and development-motivated

'slim' state-of-the-art foundry for low volume prototyping without which no global-level competency or competitiveness in design can be achieved.

- It is amply clear that **semiconductor/ microelectronics** competence needs **to be treated as strategic as nuclear energy and space technology** and that it needs to be brought under intense focus and consciously make it part of our economic planning. It is even considered to be in order for our **Parliament to hold a special session on Semiconductor/ Microelectronics** to highlight how a strong semiconductor initiative could spur economic growth.

  In keeping with this sentiment and the goal to develop technical competence and critical business to be a strong semiconductor power and position India among the **powerful nations to become part of an enlarged (S-8) Silicon Conclave,** an apex national level, not-for-profit and autonomous organization that cuts across various Government Departments/ Agencies concerned/ involved in this field needs to be formed. This could be conceptualized along the lines of say, CMC, MOSIS, IDEC, initially with 5-years funding that may be of the order of Rs.500 crores. Among others, a major mandate of this organization would be to evolve/define and periodically update a **national agenda/ roadmap for semiconductor/ microelectronics** in India with the participation of key stakeholders. Needless to mention that evolving of national agenda/roadmap would require study/ market research and intensive discussions among all stakeholders including relevant experts from Industry, R&D and Academia and that participating personnel will require to rise above their natural instincts of preserving their respective turfs.

  For the time being, the work towards this end could be undertaken by **Indian National Academy of Engineering (INAE)** through a **Forum on Microelectronics** with **patronage/ support of the Principal Scientific Advisor (PSA) to Government of India.** The Forum, in due course of time, would examine and identify the need for further restructuring of this organization including the need for creation of any new entity for effective functioning and meeting of the objectives.

  Besides the main mandate of evolving national agenda/ roadmap for semiconductor/ microelectronics, the said organization is envisaged to deal with the following specific activities:

  - Channelizing semiconductor design competence to national technological issues of various sectors and networking among academic, R&D and industrial organizations as well as working synergistically with concerned Government departments and India Semiconductor Association.

  - Facilitating, coordinating/monitoring foundry and packaging services for prototyping of designs from educational institutions and even research

organizations. This would include making available wide range of industry standard technology menu at different technology nodes with associated model parameters and design rules.

- Formulating proactively and also championing major multi-institutional project proposals, particularly where Government support is needed, and providing necessary logistic support for implementation of those projects.

Workshop Presentations

Session I : Nuances and Challenges in Entire Design Cycle

Speakers:

Aloknath De
Country Director, ST-Ericsson India Pvt. Ltd.

Anurag Seth
Managing Director (India Branch), Kawasaki Microelectronics

Rajiv Jain
Managing Director, Infineon Technologies India Pvt. Ltd., Bangalore

Presentations

1947-...Potential Realization

- Event#1: India's independence in 1947
- Event#2: Invention of Transistor by Bardeen, Brattain and Shockley. Single-transistor memory cell to millions of transistor-based solution
- Event#3: Statistical communication theory. Noise; detection theory; Information Theory
- Realizing potential

ST ERICSSON

Design Phases: Architecture, Design, Testing

- Aspect#1: Knowhow and experience variation on different phases---Customer specifications, Architecture, High-level Design, Low-level Design, Module Testing, Acceptance Testing
- Rec#1: Dealing with fuzzy environment required for Architectural phase of work; mindset change; Introduction of open problems in curriculum
- Aspect#2: Understanding market requirements and Less presence of ODM, design houses
- Rec#2: Prototypes/new product ideas; organizations having India business strategy; Application labs; Need for market creation

ST ERICSSON

Design Challenges: Hardware/software

- Aspect#3: Given an architecture, software and firmware design/optimization. Handling complex issues like hardware/ software co-design, partitioning
- Rec#3: Software content is becoming high; applying software skills to model chips. Knowledge of both for iterative design.
- Aspect#4: Fab inside/outside India
- Rec#4: Design and fab/manufacturing are quite decoupled. Fab establishment a parallel progress. Fabless approach.

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IP/SOC Design

- Aspect#5: IP Design vs SOC Design
- Rec#5: Both streams important; Depth vs. breadth need; Career path structured to incentivize people; Integration knowledge in SOC; Protocols, standards, domain knowledge for IP like USB, MIPI
- Aspect#6: Completion of full design for technology node but always following/lagging
- Rec#6: Two-pronged strategies: (i) products/applications (e.g., automotive) for stable technology node, (ii) Wide futuristic research programs leapfrogging generation

ST ERICSSON

IPR/Grants for Design: Value-based Programs

- Aspect#7: Govt. grants/aids to University/Institutions (IIT-B, IISc), SMDP
- Rec#7: Additional grant needs for research programs: low power design (clock gating, power optimization, Multi-Vt...), ultra-fast systems (GaAs, MESFET/HEMT—efficient integration of electronic and optics); Program-based initiatives and funding must.
- Aspect#8: Lack of IPR
- Rec#8: Exchange programs with other countries, Coowning IPRs, Access to IPRs, Programs like France, Singapore; National value programs

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Anurag Seth, Managing Director (India Branch), Kawasaki Microelectronics

India as Semiconductor Design Powerhouse: Nuances and Challenges in Entire Design Cycle

(Session – I @ INAE Workshop, New Delhi)

Anurag Seth

31 Oct 2009

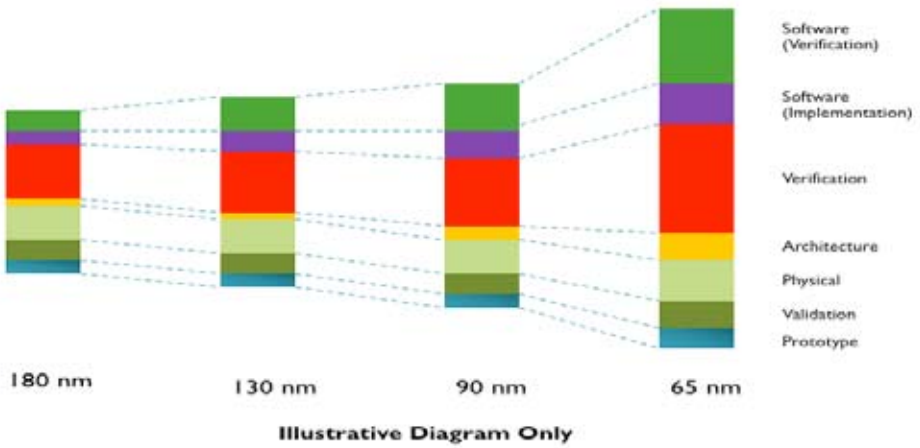
Typical Challenges/Trends in Complex SoC Designs at Advanced Nodes

- Cost of Development
  - $50M total IC R&D cost at 65nm
  - $5-10M direct respin cost per project
  - 40% of ICs exceed cost targets (Predictable design closures?)
- The SoC verification challenge
- Predictable design closure & yield ramp esp with DSM effects & variability (DFM, DFY)
  - 25% yield hit from leakage power
  - 10% yield hit from litho and process
- Need to Increase Design Productivity with increasing design complexity (>100% improvement needed per technology node for same logic content percentage)
- Power Management
- System Level Issues
  - Accurate architectural explorations at system level (esp for power and performance)
  - Package and Board level modeling
- Majority of 65nm designs will be mixed signal
  - 38% in 2007 → 80% in 2012
- SoC Test methodology

DFM (Design For Manufacturing)

	90 nm	65 nm	45 nm	32 nm
Performance & SI	✓	✓	✓	✓
Area	✓	✓	✓	✓
Power	✓	✓	✓	✓
DFY (Particle Defects)	✓	✓	✓	✓
Variation (Device + Interconnect)		✓	✓	✓
CMP & Litho		✓	✓	✓
Stress & Etch			✓	✓
Temperature			✓	✓
New Devices				✓

Verification Challenge with Increasing Design Complexity...

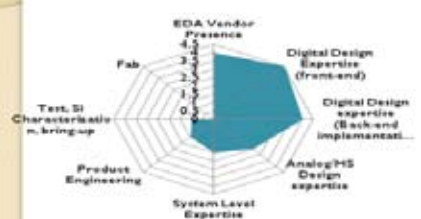


Illustrative Diagram Only

Complex SoC Design: Expertise in India

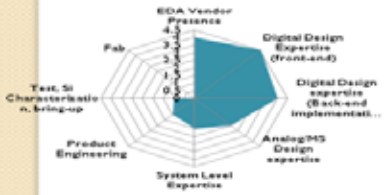
An informal crude assessment based on discussions with key people in the industry

Analog/MS Design Expertise



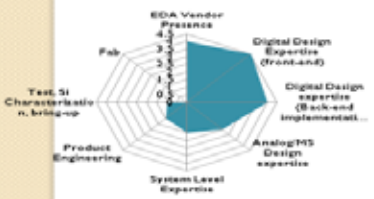
- With digital design being increasingly commoditized, analog IP's would become one of key competitive differentiators

System Level Expertise



- Most of semiconductor product designs being worked on in India are for non-Indian markets
- Very few instances of Product Engineers driving product specs from India
- Understanding and appreciation of system level specs is a key area where expertise is seen only in patches and it impacts the ability of teams in India to make optimal architectural choices
  - Package requirements, impact/simulation and choice
  - System level requirements esp for analog blocks inside an SoC
- Some companies are trying to address this gap by systematically moving some Product engineering functions to India with direct access to customers in Europe, Asia-Pac etc.

Test, Si Characterization, Fab...

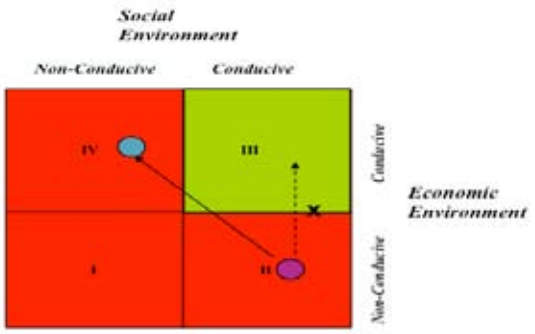


- Silicon testing, characterization and post-Si debugging
- Distance from Manufacturing (Foundries)
  - PDKs, DFM & DFY issues etc
    - EDA companies are increasingly bridging this gap
  - Indian has all the ingredients to become Fabless semicon powerhouse

Services v/s Product Mindset

"When a team in India says they're done with the design, not sure if they're really done"

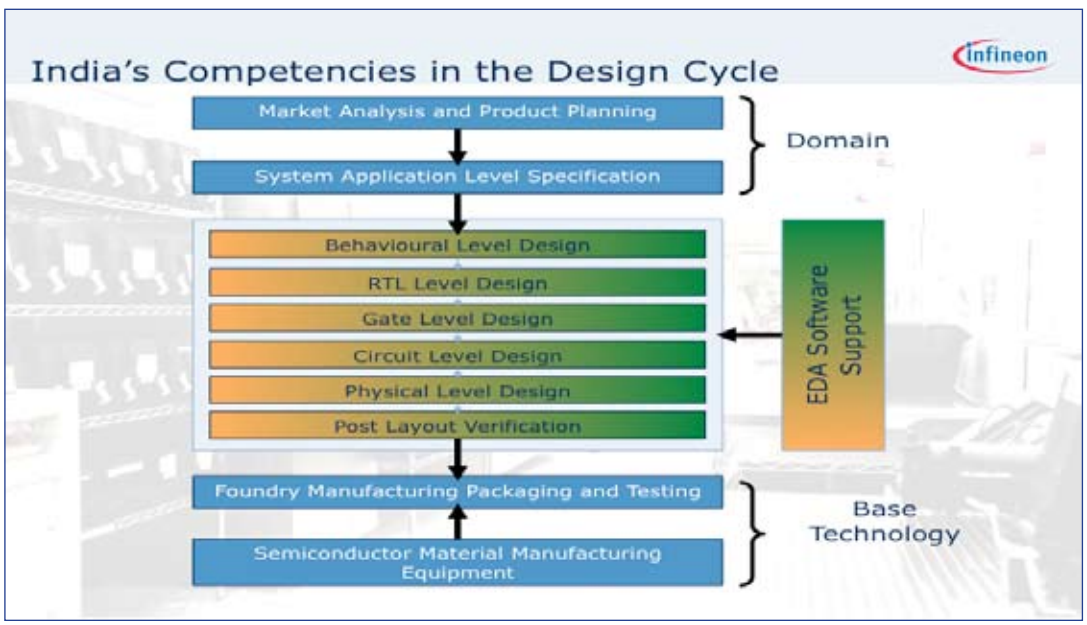
Lack of Innovation Mindset?

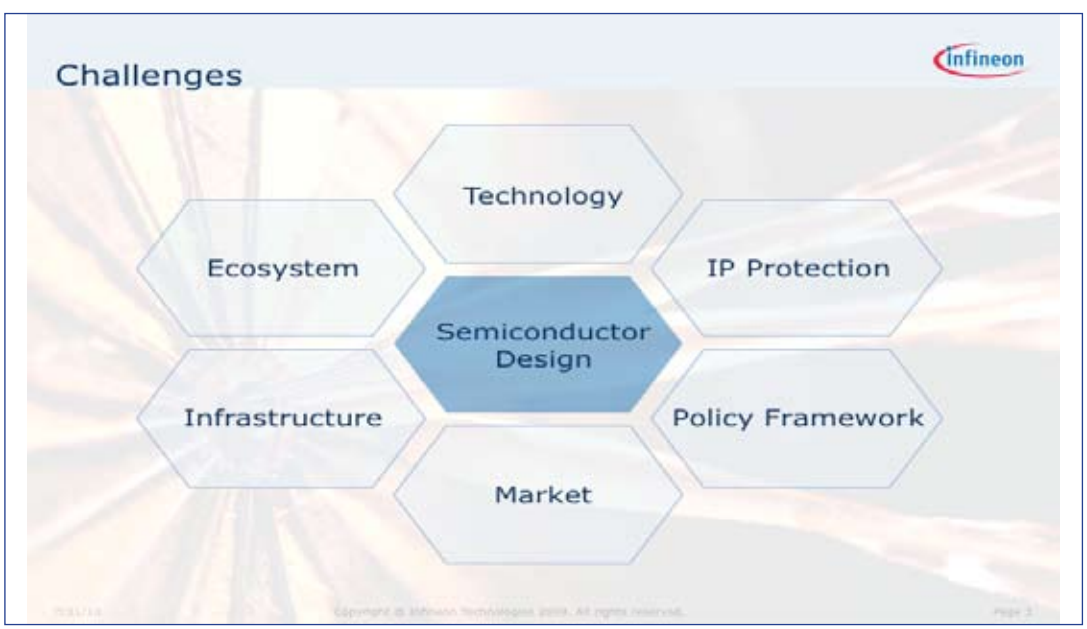


Summary

- Not having a foundry presence in India is **not** an impediment for it to emerge as a Fabless Semiconductor Design Powerhouse – most factors needed for that exist
- Some expertise/eco-system gaps surely exist as pointed out, but that has been primarily a function of services orientation in India (customer driven) and the fact that hardly any significant semicon product design is happening for India and/or is being **driven** from India
- Necessity is the mother of invention – the gap will get filled in no time as soon as there is a **necessity** created for India specific product designs at system level and/or we see innovators and young entrepreneurs bridging that mindset chasm and innovating products for Indian and even world market

Rajiv Jain, Managing Director , Infineon Technologies India Pvt. Ltd. Bangalore





Technology Challenges

- Domain Specific Nuances – Availability of domain specific inputs (Automotives, Communications, Wireless, Security)
- Architectural Issues
- Analog & RF, Digital and Power Integration in Nanoscale Design
- New Materials
- New Interconnects
- New Packages
- System / Embedded Software

Technology Challenges

- Domain Challenges
  - Domain Specific Nuances
    - Wireless Devices need Low Power, Highly Integrated, Low Cost, Low Footprint, Multi Mode, Programmable RF and Baseband
    - Automotives need Zero Defect Devices
    - Security Devices need Break Proof Technologies
- Architectural Issues
  - India is a large market without dominant domain specific players
  - Market related inputs originate outside India. Dependency upon good global collaboration; Limited "End-Product" mindset
  - Smaller Pool of Concept Engineering, System Engineering and Application Engineering

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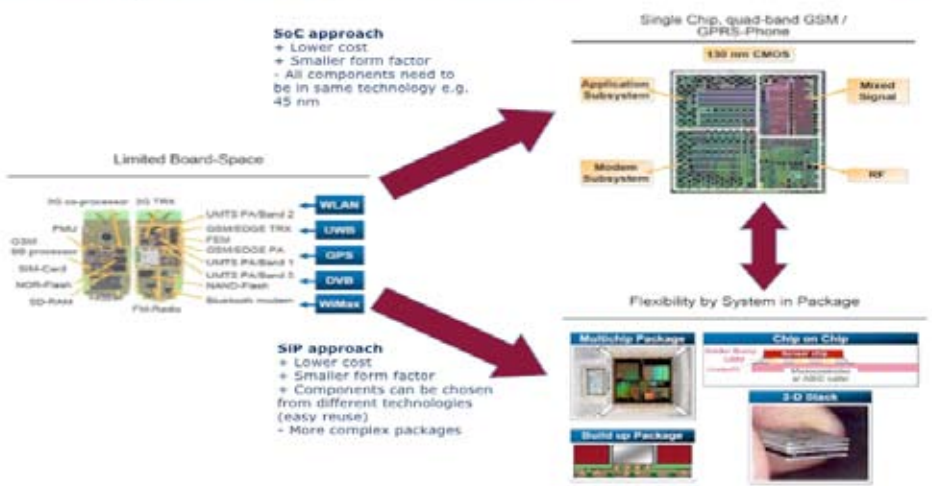
Integration of Multiple Functions & Conflicting Technologies at Right Price Point



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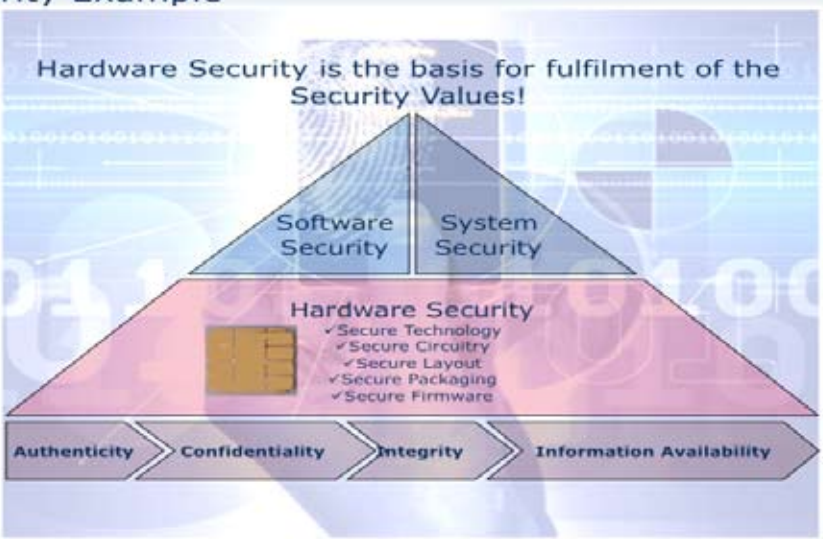
Security Example



Why Zero Defect Design?

Supplier → Semiconductor Manufacturer → Tier 1 Supplier → OEM → End customer

Example : Cost Explosion in case of a supplier quality event

Failure analysis	Failure analysis Cost of Scrap	Cost of Scrap Cost of Overtime	e.g. 1 day linedown Controlled shipping	e.g. recall of 10,000 cars
~ 10 k€	~ 50 k€	~100k€	~1000k€	~10000 k€

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Device Level Challenges: Low Operating Voltage

- Supply vs. Threshold Voltages as a function of technology nodes
- Drive Current vs. Leakage Current as a function of technology nodes
  - Lower VDD, Lower Vt, higher leakage
  - For same performance at lower VDD, threshold voltage Vt should be reduced
  - As Vt is lowered, drain-source leakage increases exponentially, thereby increasing standby power.
  - Thus various flavors of the technology are needed for different applications.
- Transistor Intrinsic Gain vs. Transit Frequency
  - As gate length decreases, intrinsic gain of the transistor decreases due to higher channel length modulation
  - Though fT increases with lower gate length, the advantage is offset due to lowered intrinsic gain.
  - Analog designs do not get advantage of technology shrinking.
- FUSI, High-K and Strained Silicon, or new devices such as FINFET

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Market Pressures

- Price / Performance
- Form Factor
- Feature boom (Must have vs. Good to have)
- Environmental Pressures
- Local End Consumer Industry (Limited Local consumption) - Technology Orientation vs. Service Orientation

IP Protection

- Global Collaboration vs. Export control (Seamless / borderless technology access)
- Legal control and time lost (Time-to-Market) in technology access
- Legal Quagmire (Human/ Geopolitical imperative of technology)
- Local IP protection regime

Other Challenges

- Infrastructure
  - Semicon Ecosystem imperatives for seamless collaboration
    University Infrastructure for Semicon Design
  - Equipment, Technology, Jobs in Base Technology
  - End Product Ecosystem and manufacturing mindset
- Policy Framework
  - Government Support e.g. ITRI-TSMC

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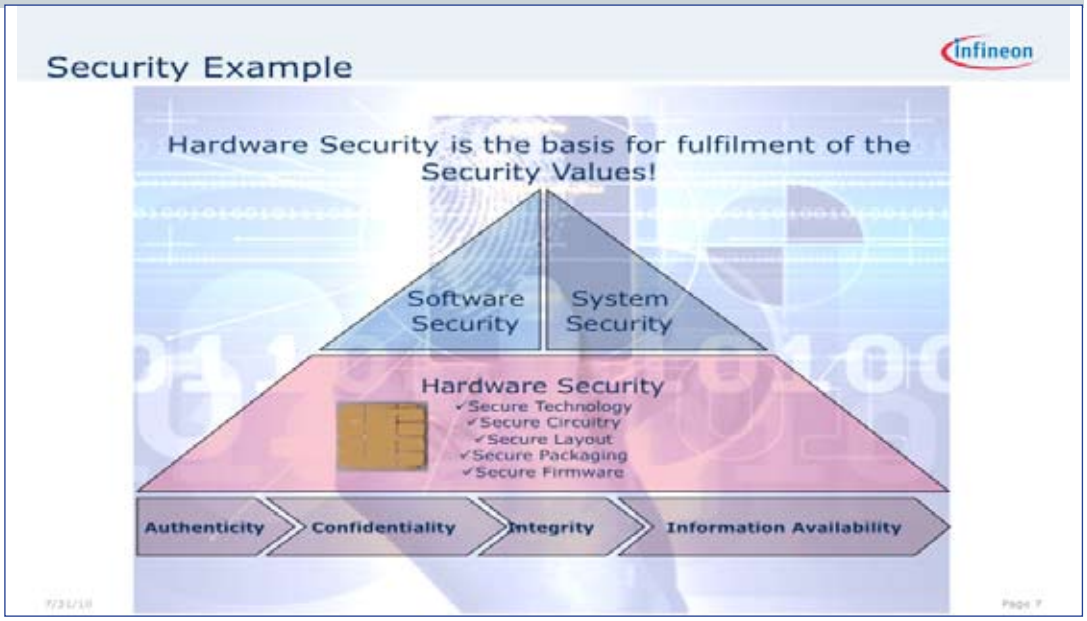
Security Example
Infineon
Hardware Security is the basis for fulfilment of the Security Values!
Software Security
System Security
Hardware Security
✓Secure Technology
✓Secure Circuitry
✓Secure Layout
✓Secure Packaging
✓Secure Firmware
Authenticity
Confidentiality
Integrity
Information Availability

Session II : Killer Applications and Products in India Context

Speakers:

Ganesh Guruswamy
Vice President & Country Manager, Freescale Semiconductor India

P. Sridhar
Sasken Communication Technologies Ltd.

Rajeev Shorey
President, NIIT University

Vivek Sharma
Head – India Operation, STMicroelectronics Pvt. Ltd., Greater Noida

Presentations

Ganesh Guruswamy, Vice President & Country Manager, Freescale Semiconductor India

October 31, 2009

Killer Applications and Products in India Context

Ganesh Guruswamy
Vice President & Country Manager
Freescale Semiconductor India

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Why?

- We are different; our needs are different
- Market Revenue
- Growing Rural Market
- Growing Middle Class & Urban population

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India's Growing Need

- Power
- Healthcare
- Education

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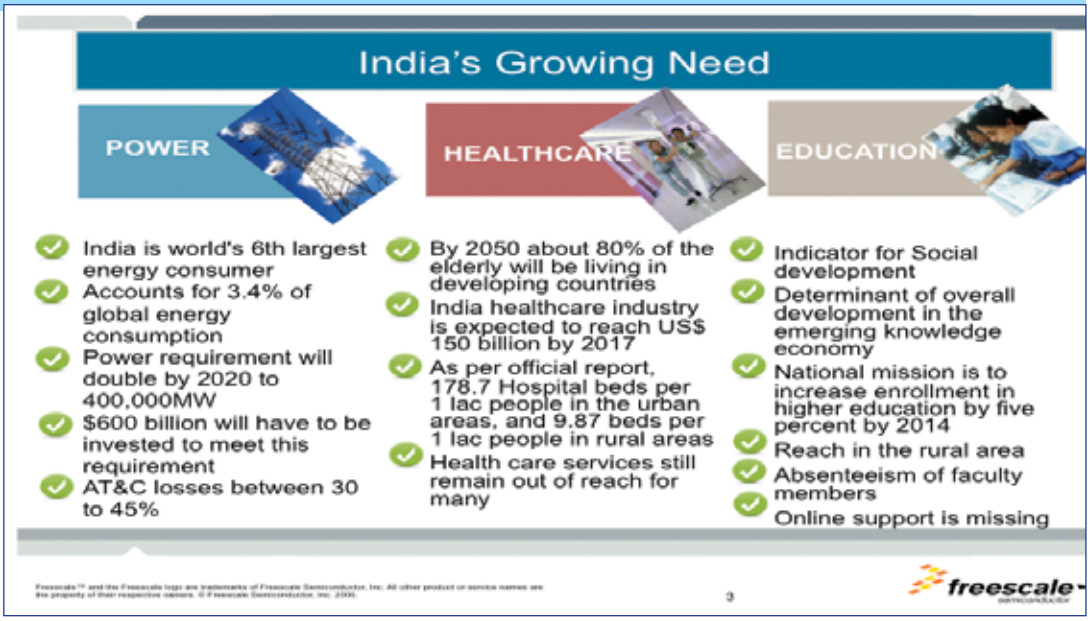
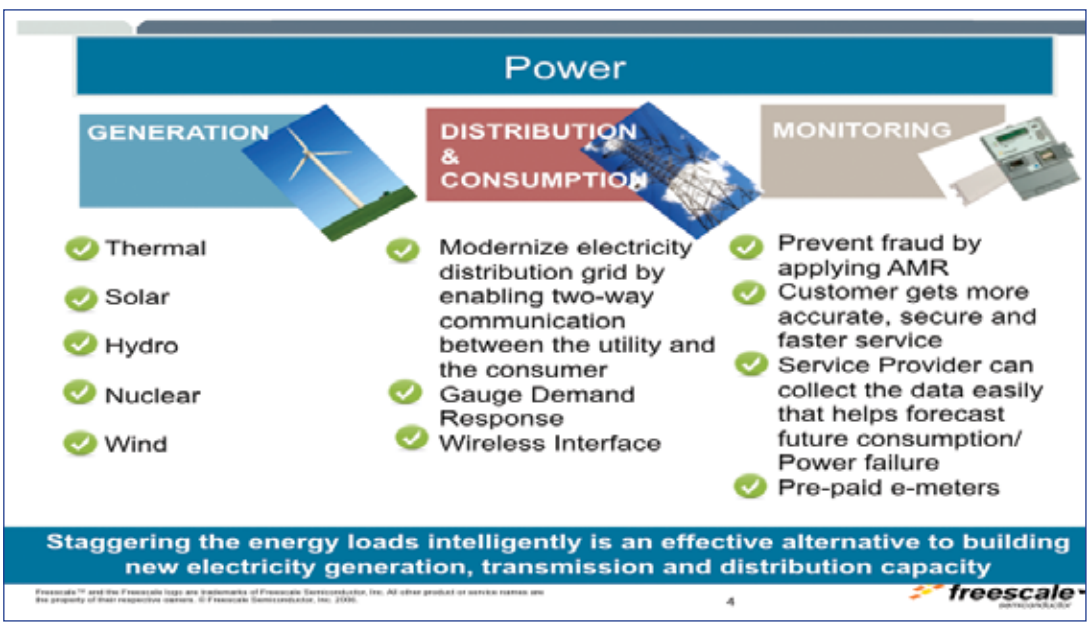
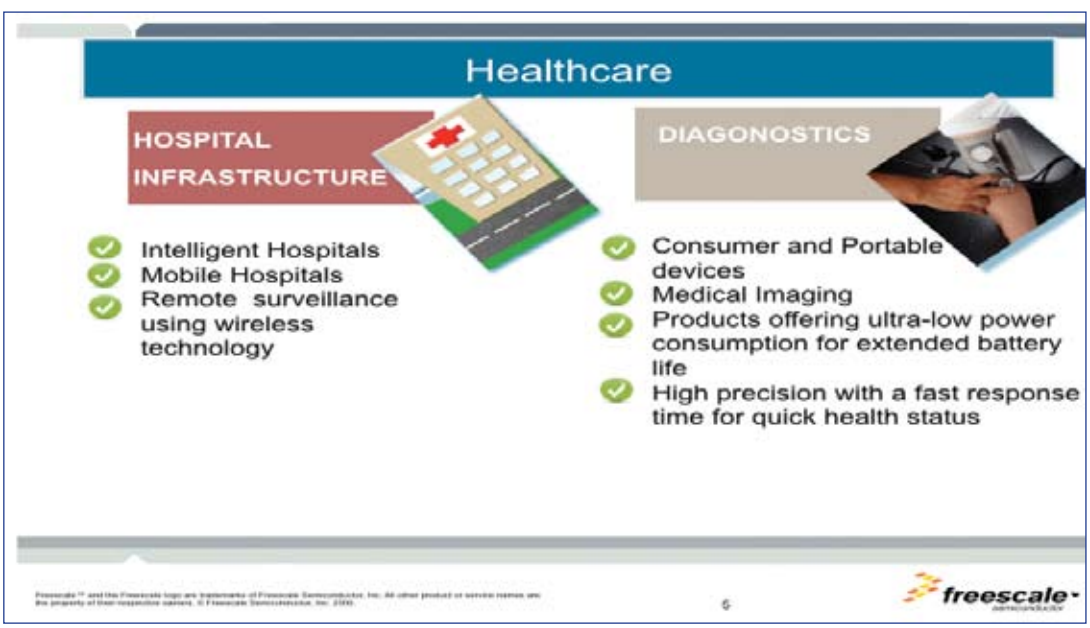
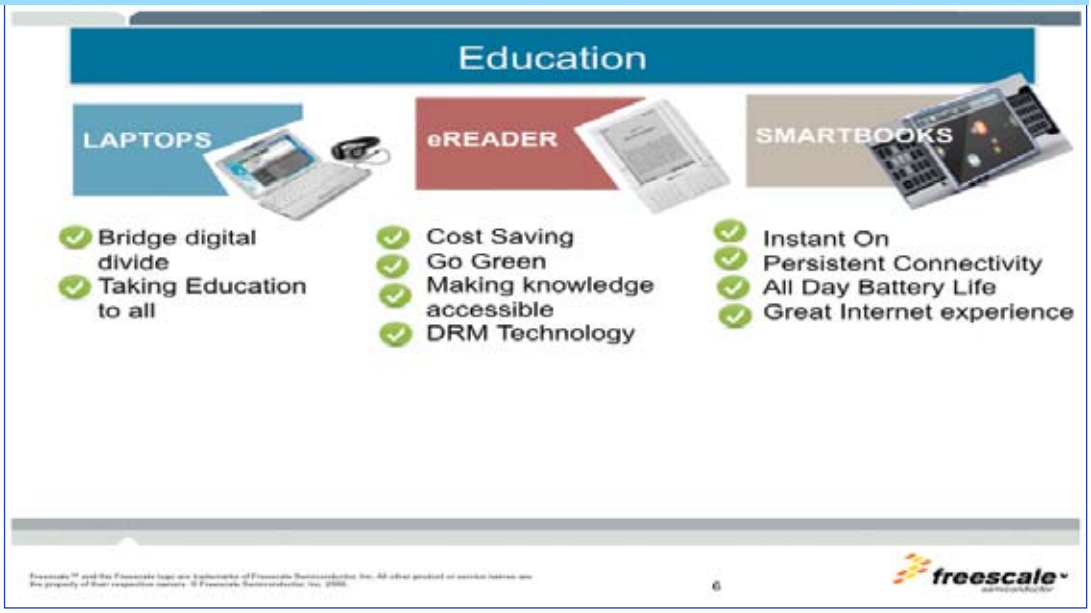
Ganesh Guruswamy, Vice President & Country Manager, Freescale Semiconductor India








Education
LAPTOPS
eREADER
SMARTBOOKS
Bridge digital divide
Taking Education to all
Cost Saving
Go Green
Making knowledge accessible
DRM Technology
Instant On
Persistent Connectivity
All Day Battery Life
Great Internet experience
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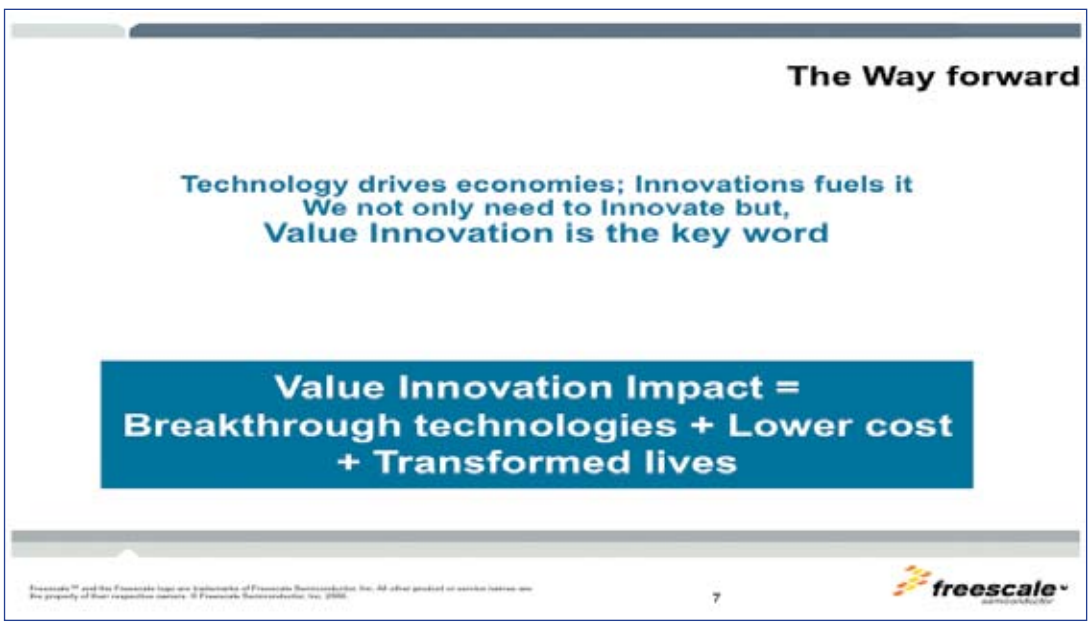
The Way forward
Technology drives economies; Innovations fuels it
We not only need to Innovate but,
Value Innovation is the key word
Value Innovation Impact =
Breakthrough technologies + Lower cost
+ Transformed lives
7
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Market Perspective

India is one of the Fastest Growing Electronics market in the World

- India's electronics market stands at $6 billion, is expected to be more than $10 billion by 2012.
- Indian semiconductor market has grown from about US$ 2.1 billion to about US$ 4.1 billion in the last 4 years and expected to reach US $ 9.8 Billion by 2012?

  (Assumes Linear trend, no disruptive change in supply chain

  What if manufacturing aligns with end markets?)
- India accounted for 1.3 per cent of the global semiconductor revenue in 2007

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Market Perspective

Growing demand for IT hardware, office automation products, and consumer electronics products such as mobile phones, etc., is spurring the demand for semiconductor and a full-fledged semiconductor ecosystem in India.

Key Segments in the Semiconductor Application Market

Telecom	44%
Office Automation	32%
Consumer	7%
Industrial, Automotive and rest	17%

Interesting Application Segments

Healthcare

health tourism, clinical trials (testing of instruments/

Energy

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Healthcare - Need, Market & Solutions

Problem Statement	Market	Solution/s	Challenges
Treatment of chronic or long term conditions (asthma, diabetes, etc.)	Short range point-to-point communication technologies	**Bluetooth, NFC**	Security, Reliability & Interference Power Budget
The need for **"worried well" to better manage and monitor** their general health	Periodic/Real-time readings to be centrally gathered from around the home and a coordinated picture of overall health indications to be delivered	**WiFi, Bluetooth**	Simple pairing and connection is a major challenge that wireless system designers need to overcome - devices need to work straight out of the box through a single click.
Counterfeit drugs industry in India pegged to be at Rs.40,000 crores	An increasing need to know more on "what we buy"	**RFID, Holograms, Anti-counterfeit scanners**	Counterfeiters' ability to reproduce holograms and other sophisticated printing techniques has dramatically improved between 2001 and 2005 High cost of technology
The need for supportive technologies to enable the **person/patient to live independently in their home**	Market for remote personal health monitoring will reach $5 billion in 2010 Will explode to $34 billion by 2015 [Source: Forrester Research]	**Wireless mesh network technologies**	Engaging the elderly with New Technologies

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Challenges

- Ensure interoperability between health monitoring devices and home-based hubs that relay the data from the devices to healthcare providers
- Regulatory compliance and malpractice
- Lagging IT infrastructure on the back-end
- Structural barriers to adoption
  - the present ill-defined reimbursement schemes and
  - the need to integrate wireless home health systems with clinical workflow processes
- Emphasis is now on wireless system designs that offer the tools to create new and innovative medical products to address this rapidly growing market

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Complexity lies in "Enabling It"

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Killer Applications and Products in India Context

Rajeev Shorey (Ph.D, FNAE)
President, NIIT University
www.niituniversity.in

INAE Workshop, 31 October, 2009

Statistics: Healthcare Sector

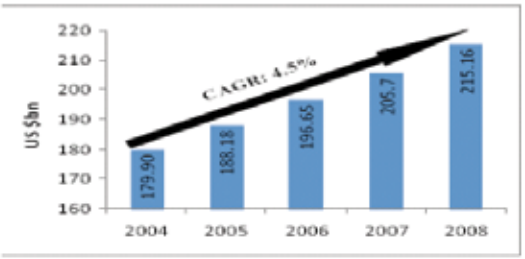
- India's healthcare sector has been growing rapidly
- Estimated to be worth US$ 40 billion by 2012
- Revenues from the healthcare sector account for 5.2% of the GDP
  - Third largest growth segment in India
- The Indian healthcare industry is expected to become a US$ 280 billion industry by 2022

Ref: Pricewaterhouse Coopers report, 'Healthcare in India: Emerging market report 2007'

Investments in the Healthcare Sector in India

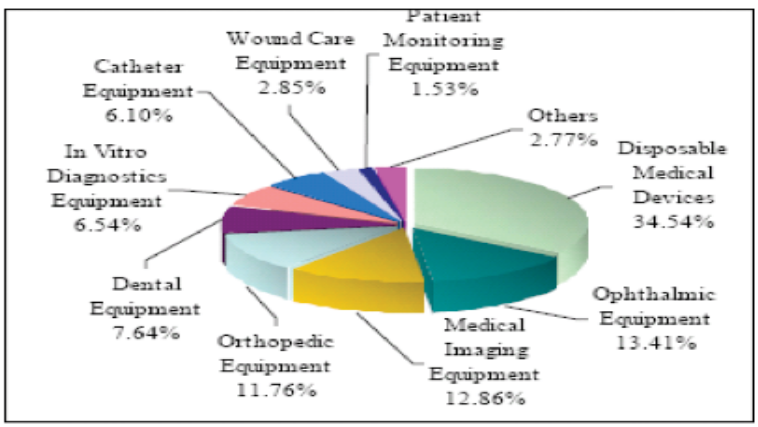
- Medical care services provider Apollo Hospitals group will invest about US$ 235.69 million in the next 18 months to set up 15 hospitals in tier-II and tier-III cities in India
- The Indian government plans to invest US$ 177.22 million across the golden quadrilateral (GQ) project, to develop nearly 140 trauma care centres on the 6,500 km long north-south and east-west corridors
- Fortis Healthcare Ltd will add 28 hospitals to its 12-hospital chain by 2012
- George Soros's fund Quantum and BlueRidge bought 10 per cent in Fortis Healthcare
- Manipal Health Systems raised over US$ 20 million equity from IDFC Private Equity Fund
- Bangalore-based HealthCare Global Enterprises raised over US$ 10 million in equity from IDFC
- Metropolis Health Services, a diagnostic chain, raised over US$ 8 million in equity from ICICI Venture
- Investment firms Apax Partners, IFC and Trinity Capital have invested over US$ 200 million in hospital firms

Global Medical Devices Market



Global Medical Devices and Equipment Market

Segmentation of Global Medical Devices & Equipment Market – By Geography



Segmentation of Global Medical Devices & Equipment Market – By Applications

Indian Medical Devices and Diagnostic Industry: Growth Drivers

- The growth of Indian medical devices and diagnostics industry is driven by a host of factors
  - Booming Economy
  - Increasing Healthcare Expenditure
  - Changing Demographic Profile
  - Increasing Incidence of Lifestyle Diseases
  - Increasing Number of Medical Tourists
  - Proliferation of Hospitals

Technologies for the Healthcare Sector

- "Technology is to healthcare what nervous system is to human body"
- Key Trends
  - Convergence of Consumer Products with Healthcare Products
    - Cell phone is going to become a health management and monitoring device
  - Miniaturization of Medical Devices
    - Convenience
    - Low power
    - Low complexity
    - Affordable (if "scaled")

Main Applications in Healthcare Sector

- Blood pressure meters
- Glucose meters
- Digital thermometers
- Pulse oximeters
- Respiratory aid
- Inhalators
- Cholesterol meters
- Portable ultrasound
- Insulin pumps
- Data loggers
- Alcohol meters
- ...

Miniaturization of Medical Devices

Pulse Oxymeter

Portable/Handheld Pulse Oxymeter

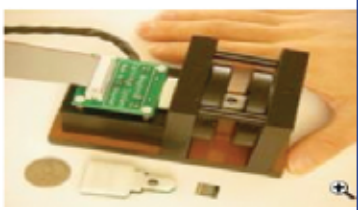
Handheld ECG

Glucose Monitors for Diabetes

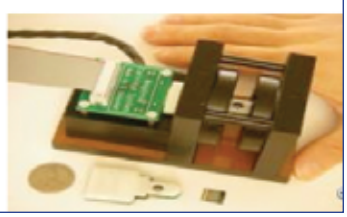
Technologies for the Early Detection and Diagnosis of Killer Diseases

Bio-Detection Chips

- Device that can scan blood and find signs of cancer, even at its earliest stages
  - Stanford Researchers
- Early detection will allow early treatment and greatly improve the survival chances of patients



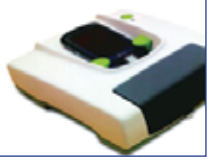
- The detector contains a silicon chip
- The chip contains 64 embedded sensors that monitor magnetic field changes
- To these sensors are "capture antibodies" which trap specific cancer-related proteins as they pass through the sensor with the blood



BigTec's Point-of-care Diagnostic Kit

Lab on a Chip

- Point-of-care-devices are gaining popularity
- BigTec planning to launch a diagnostic kit to detect Hepatitis B infection using DNA recognition technology
  - The kit can detect the pattern of the virus and provide an exact result within 15–20 minutes of a test
- BigTec is working towards developing similar kits for other infectious diseases, such as chikungunya, malaria and dengue



The Use of Smart Cards

First Recipient of the RSBY Card

Rashtriya Swasthya Bima Yojana Scheme

Core Recommendations

- Healthcare: from a State subject to Centralized subject
- Providing Affordable Healthcare to All
- Accreditation and Standardization
- High Import Duties: Escalation in the Cost of Medical Devices
- Hurdles Faced by Indigenous Companies in Making High-End Equipment
- Cultivating an "Export Mindset" by Indigenous Manufacturers

"Out-of-the-Box" Thoughts

- Mobile Clinics
  - Equipped with state-of-the-art equipments
  - Has the potential to scale in India
- Exploit synergy of Healthcare Sector with the Automotive sector !

Mobile & Portable Medical Solutions

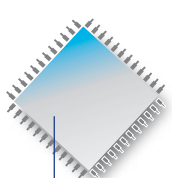
- Factors that are boosting the market of mobile and portable medical solutions
  - Shortage of facilities
  - Aging population
  - Rising hospitalization costs
- Today's medical electronics provides a number of portable diagnostic devices
- Keeping people out of hospital is also key to controlling healthcare costs
- Handheld instruments are a solution
- These portable solutions require low power consumption, low voltage and small size

A Telemedicine Cart

AFHCAN Telemedicine Cart

"The advent of telemedicine has completely changed the quality and accessibility of rural ENT healthcare.

Philip Hofstetter, Audiologist



Vivek Sharma, Head – India Operation, STMicroelectronics Pvt. Ltd., Greater Noida

Road to Powerhouse in Semiconductor Design: A Perspective

- Engineering Availability at Cost-competitiveness
- Young Engineering, Basic Design Implementation
- Credibility, Skilled Engineering, Advanced Design Implementation
- Access to Market, Anticipating Needs, Defining Products, Product Design
- Innovative Designs, Design Powerhouse

Session III : Competencies for World-Class Chip Design

Speakers:

A.B. Bhattacharyya
Emeritus Professor, Jaypee Institute of Information Technology, Noida

P.P. Chakrabarty
Professor & Dean (Sponsored Research & Industrial Consultancy),
Indian Institute of Technology, Kharagpur

Jyotirmoy Daw
Managing Director, Mentor Graphics (India) Pvt. Ltd., Noida

Presentations

A.B. Bhattacharyya, Emeritus Professor, Jaypee Institute of Information Technology, Noida

Making India Powerhouse for Semiconductor Design

A. B. Bhattacharyya
Emeritus Professor

Jaypee Institute of Information Technology, Noida (Deemed University)

Outline

- Manpower: India's Demand/Supply Profile
- Benchmark: G7 Univ. Design Competency
- G7 Silicon Design Initiatives
- G7 Silicon Design Initiative Charters
- Curriculum Engineering
- Univ. Design Capability: Way Forward
- Roadmap: G7 Model

Manpower: India's Demand/Supply Profile

Demand Profile

- Requirement for Software and Hardware Engineers over last five years around 7 million
- Approximately 10,000 VLSI designers in place
- A demand chain of 125 Enterprises/Companies
- Majority are design service providers following time-tested, low risk, cost effective IT sector model
- Estimated market for design-service related activity: 750 million dollars
- Strong indication of upward movement in job profile from service to circuit design

Manpower: India's Demand/Supply Profile (cont.)

Supply

- 1500 Engineering institutions with annual turnover of 0.2 million CS/EC Students
- Industry assessment: (25–30)% considered employable
- 1.2 lakh faculty: majority with poor R&D track record

VLSI Design specific Govt. Intiatives

- 32 centers supported by Ministry of IT under SMDP program in VLSI design
- 46 centers supported by ADA under NPMASS program for MEMS Design

Benchmark: G7 Univ. Design Competency

Country	Period	Design Prototyped	Tech. Node	No. of Univ.
CANADA	2007	378	65 nm	3000 (s)
CHINA[1]	2007	48	90 nm	20 (u)
EUROPE	1982–2007	3,654	95 nm	195 (u)
JAPAN	2007	433	0.18 µm	55 (u)
KOREA	1995–2008	1,814	0.18 µm	60 (u), 3700 (s)
TAIWAN	1992–2008	9,044	90 nm	80 (u)
USA	1981–2008	12,500	65 nm	50,000 (u)
INDIA	2002–2009[2]	50-60	0.18 µm	5 (u)

1 CHINA-STM Tie-up for 65 nm technology for university chip design
2 extrapolated

Benchmark: G7 Univ. Design Competency (cont.)

- Annual ≈ 25% ↑ in no. of chips, and 15% ↑ in no. of Universities for prototyping
- Annual low complexity, concept validation chips from University Fab
  - USA: (10–15): ≈ 300
  - EUROPE: (6–10): ≈ 300
  - JAPAN: (3–5): ≈ 100
- For VLSI education design, printing on silicon considered indispensable

G7 Silicon Design Initiatives

Country	Organisation Created	Year
CANADA	Canadian Microelectronic Corp. (CMC)	1984
CHINA	Integrated circuit design (CICC)	2000
EUROPE	Europractice/Circuit-Multi-Project (CMP)	1981
JAPAN	VLSI Design & Education Center (VDEC)	1996
KOREA	Integrated Circuit Design Education Center (IDEC)	1995
TAIWAN	Chip Implementation Center (CIC)	1992
USA	MOS Implementation Service (MOSIS)	1981

G7 Silicon Design Initiatives (cont.)

- Not-for-profit organisation
- Govt/Industries/Universities/Professional Societies, etc., as stakeholders
- For chip design education and research: required superspecialization support and coordination provided
- Design focus:
  - system-centric → SoC → system expertise
  - circuit-centric → CoS → design-on-silicon expertise
- EDA: standardization, interface

G7 Silicon Design Intiative Charters

- Coordinates Fabrication/Design/Testing services
- Provides system-level prototyping stations on FPGA for SoC/Embedded application
- Creates national design network and project bank
- Prototyping support for design courses at negligible cost
- Fosters Industry–Academia two-way collaboration
- Expatriate participation, and international collaboration
- Educational activity balance sheet: IDEC (KOREA) 1995–2005: 60 (Univ.), 389 (Prof.), 3700 (Students), 62 (WG), 6 (Reg.Cent.), 38 (Books), 245 CD-ROM, 2,222 (L/S), 61,554 (Part.)

Curriculum Engineering

- Specialisation not in Microelectronics/VLSI alone
- High degree of emphasis on application domain
- Design prototyping program on silicon testing telescoped in three semester Master's program as:
  - Project formulation: 3 months
  - Specification/Architecture: 4 months
  - Design/Simulation/Layout: 5 months
  - MPW Fabrication/Documentation: 3 months
  - Testing/Breadboarding: 3 months
- Challenges: Mapping of Industrial culture in academic enviornment; design flow management as assembly line

Curriculum Engineering (cont.)

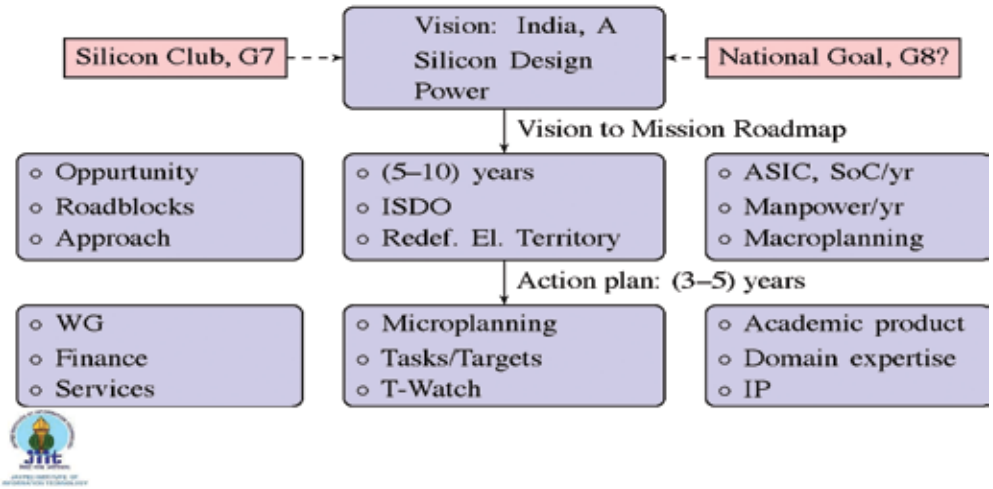
- Annual budget ≈ Rs. 10–12 lakhs: prototyping (10–15 designs)
- Professional support for EDA tools management
- Faculty time: 3–4 man-month/project
- Participation of System House, Design House, IP vendors, CAD tool supplier and PCB Manufacturer
- PhD program ⇒ research chip, MS program ⇒ industrial chip
- Working chip: A degree on Silicon!
- VLSI chip design education is costly, ignorance is much costlier

Univ. Design Capability: Way Forward

- Silicon design sovereignty is as vital to India as sovereignty over print media
- Indigenous project bank
  - national security, nuclear, and space programs
  - communications
  - health care, environment, etc.
- Institution base (+), domain expertise (-)
- External foundry service—reliable
- Specialised support services—weak link
- Master's program: industry/user sponsorship for manpower and projects

A.B. Bhattacharyya, Emeritus Professor, Jaypee Institute of Information Technology, Noida.

Roadmap: G7 Model



Mission Launch Strategy: India Specific Design/Products

Category-1: Industry Product

- System-on-Chip (SoC)/ASIC designs: ≈ 6
- Application domains: defence/security, communications, healthcare, transportation, consumer, energy, etc,
- Participation: govt-private-universities, expatriates
- Time Frame: project specific (one to three years)
- Attributes: intellectual property, volume production, market competetive

Category-2: Technology Demonstration Product

- Design, simulator package at cutting edge

Why Prototyping Indispensible in VLSI Design Education

- Involves team effort
- Requires industry involvement
- Provides skill for System and Silicon complexity management
- Gives insight of potential and limitation of EDA tools
- Creates awareness of current technology, market dynamics, and VLSI economics
- First-pass successful prototyping: engineer's 'EUREKA MOMENT'
- Intellectual property and entrepreneurship

P.P. Chakrabarty Professor & Dean (SRIC),Indian Institute of Technology, Kharagpur

Making India a Powerhouse in Semiconductor Design: Competencies for World Class Chip Design

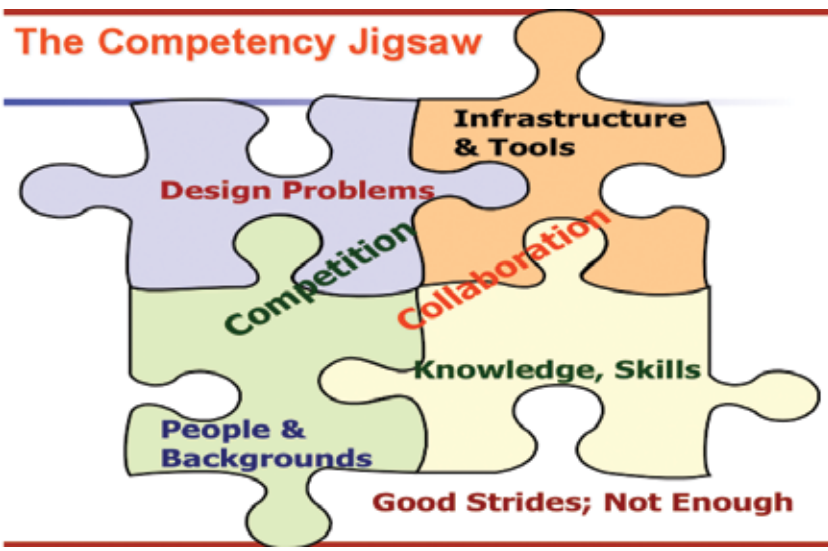
Presented by:

Dr. Partha P Chakrabarti
Advanced VLSI Design Lab
Dean (Sponsored Research & Industrial Consultancy),
Indian Institute of Technology
Kharagpur 721302 India

PPC IITKGP

1

The Competency Jigsaw



Good Strides; Not Enough

PPC IITKGP

2

The Competency Challenge for India

Ultra, Mega, Integrated: low power, size, cost; high volume, robust, reliable systems

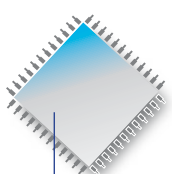
Tools for non-EECS people, High-Speed Prototyping, Fab support

Beyond EECS: All Core Engineering, Biology & Medicine,

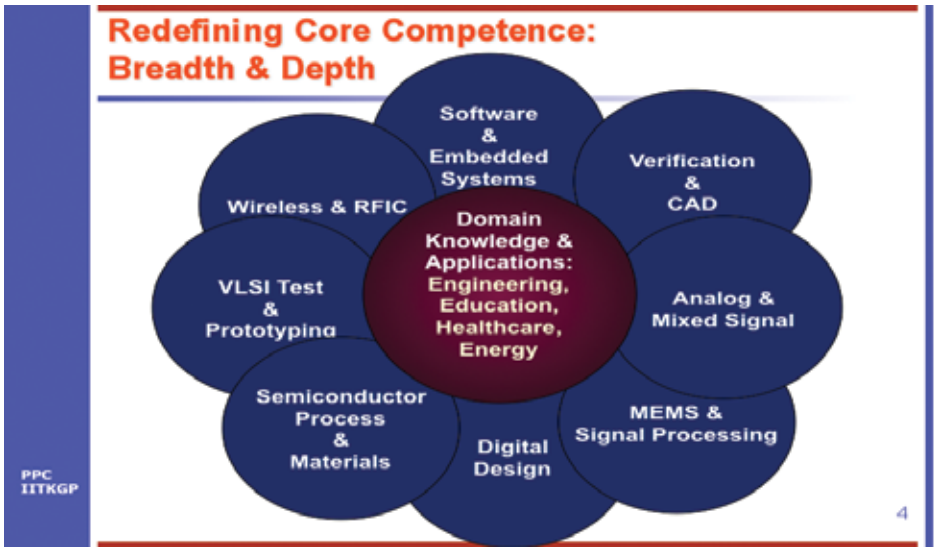
Wide Breadth, Sufficient Depth, Skills Plus Domain Knowledge

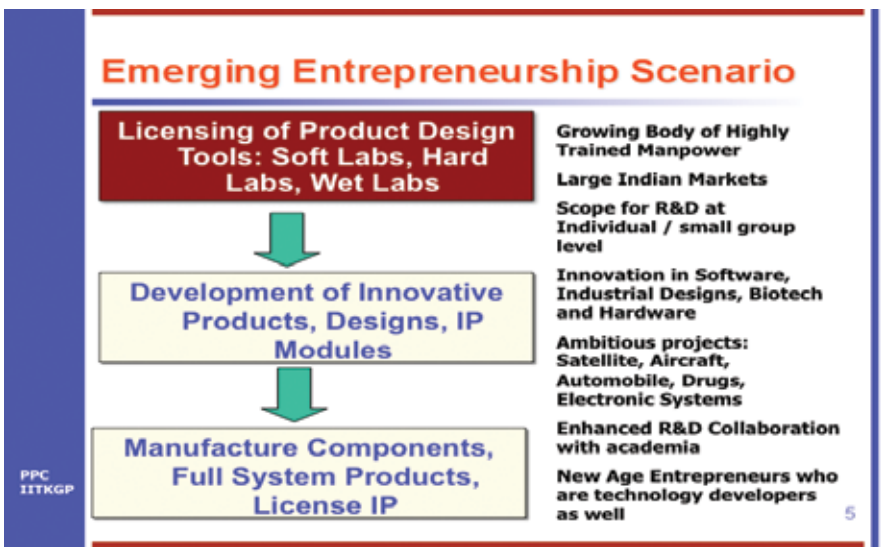
PPC IITKGP

3



P.P. Chakrabarty Professor & Dean (SRIC),Indian Institute of Technology, Kharagpur



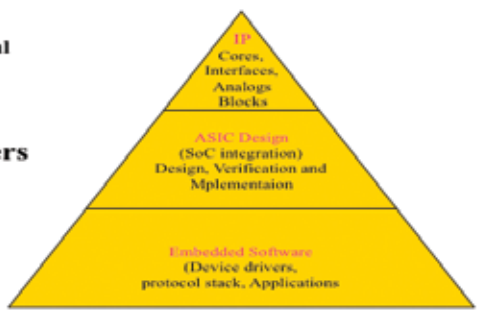



The Next-Gen VLSI Competency Mission
• Lies in solving our own design challenges by our own people in our own country.
• Redefine India's Core Competence Requirement in Terms of Quality and Quantity, Make a spreadsheet and set up a Mission to achieve the same.
• For this we need to address the following aspects of Competency
– Designs: Processors, Laptop, Phone, Chipset
– Applications: Engineering, Education, Healthcare, Energy
– Tools: Enable-all approach in addition to specialized engineer approach
– Knowledge & Skills: New ICT-based, academia-run, industry-supported programme
– Huge Repository of Everything
• Coherent Integration of Federated Approaches of Industry-Academia Programs
PPC IITKGP
7

Jyotirmoy Daw, Managing Director, Mentor Graphics (India) Pvt. Ltd., Noida

Chip Design Hierarchy

- **Today's Market Drivers**
  - Netbooks/Smart Phones/Digital TV/Gaming devices/STB
  - Mostly digital processing
  - Lots of software
- **Tomorrow's Market drivers**
  - Embedded Internet devices
  - Wearable computers
  - Smart Phones with desktop functions



Have we acquired all the competencies and skills ?

- **We are the "Design" factory**
  - Over 200 Design houses
  - 22 out of top 25 Design Houses have presence in India
- **We are the "Users"**
  - Over 75000 engineers employed
    - VLSI Design – 11%
    - Embedded Software – 82%
    - Board Design – Rest
- **Competencies and Skills -**
  - Implementation is our strength
    - From Spec to tape-out
    - Languages/Methodologies/Tools
- **Product or Technology Innovation is not our forte**

Does our domain expertise match with market requirements and dynamics ?

- We are OK for now
  - SoC means more Integration
    - Less of Design and more of Verification
    - Unique opportunity here with Verification
      - Requires learning new language/methodologies and Tool
      - Easier for fresh people to learn them
  - More Software content
    - Less of custom hardware and more of Processor Cores
    - Embedded Software – again a strength for Indian industry
- Future ?
  - More Analog IPs will be created
    - More art than automation
    - Area where we need to pay attention

Mentor Graphics Confidential Page: 4 Mentor Graphics

How do we steer better our University programs ?

- Tier I Universities
  - Focus on Technology Innovation
  - Needs significant investment
    - To establish competency centers
    - To attract the best minds
    - Partner with Fabs
- Tier 2 Universities
  - Will need to produce hirable engineers (without further training)
  - Need to focus on training the basic Language skills
    - SystemVerilog for hardware Design
    - Matlab and C/C++ on Embedded OS for Embedded Software
  - More practicals than Theory - Need to build Labs with Tools
  - Hire people from the industry who know how to use the Tools
  - Partner with specific companies
  - Universities should establish campus close to where the industry is

Mentor Graphics Confidential Page: 5 Mentor Graphics

Session IV : Leveraging on Design Ecosystem

Speakers:

Rajat Gupta
GM–India Operations, Beceem Communications Pvt. Ltd., Bangalore

Sunil Sherlekar
Founder & Head of Research, Computational Research Labs. Ltd.
& Chief Scientist, Tata Consultancy Services Ltd., Bangalore

Jaswinder Ahuja
Corporate Vice-President and Managing Director, Cadence Design Systems India Pvt Ltd., Noida

Presentations

Rajat Gupta, GM–India Operations, Beceem Communications Pvt. Ltd., Bangalore

BECEEM

Are we leveraging India's Design Eco System?

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Background

- India is now the preferred destination for IC design and SW development outsourcing services
  - Service is defined as an economic activity that does not result in *ownership*
  - A thriving service industry implies a large design work force: but do we know all it takes to build a *product*?
- India's 50M+ middle class can easily become the preferred target for all product companies in the World
- Why are there no Indian semiconductor product companies?

BECEEM

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Measuring Effectiveness

- How can we know if we are effectively leveraging the design Eco-system?
  - Start-ups are formed in India with a product delivery business model and planned financial exit through India's stock market
  - Venture Capitalists create funds for India and actively pursue entrepreneurs in India for investment
  - A semiconductor product company (includes EDA) gets listed in India & gets comparable valuation
  - Companies building end products (automotive, consumer, control, healthcare, security) co-develop and procure semiconductors from Indian semiconductor product / service companies. .

How can we institutionalize:
Independent Forecasting, Measuring and Tracking of Metrics?

BECEEM

Rajat Gupta, GM – India Operations, Beceem Communications Pvt. Ltd., Bangalore

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The Eco System Components

- Design Know How: Deficiencies & Barriers
  - Chip Design
    - Test: Poor Standalone biz viability → insufficient Capex
      - Is there a hidden opportunity here?
    - Product Qualification: Curricula don't address "economies of scale"
    - Failure Analysis: Create Govt funded infrastructure
      - How to ensure it does not get fossilized over time?
      - Need to have an R&D focused on FA & measurement techniques around which the lab gets set up
  - Regulatory
    - E-Waste management
    - SAR and other specs. . . Compliance spec; measurement; approval?

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The Eco System Components

- Learning & Adopting New Technologies ***Early***
  - Harnessing cross-functional skills
  - MEMS: Modelling, tools, design, applications, integration
  - CNT: "hammer in search of a nail"
  - Photo-voltaics: Where are the applications?
  - Display Technologies:
    - Solid State lighting: Plenty of room at the top
      - Currently best technology ~ 100 lm/W; Physics limit ~ 683 lm/W
    - (OLEDS) R&D "know-how" → Industry
- Creating new technologies. . .
  - IPR related legal issues not solved generically
    → barriers to inter-institutional collaboration
    → missed opportunities in technology creation
  - Participate in standards creation in every technology area

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The Eco System Components

- Legal & Financial Models (to consider and adopt?)

- Early stage Start-ups (UK: SBRI):
  → Govt maintains a list of Start-ups funded by one or the other of Govt schemes and allow them competitive access to Govt R&D Contracts DRDO / ISRO/ other Govt R&D Institutions

- Encouraging R&D in established companies (SQ: RISE)
  → Companies with R&D intensive product development can claim Govt Funding proportional to R&D expenditure subject to T&C.

- Other Incentives (SQ):
  → Tax exemption for 1st Rs X of revenue. T&C apply.
  → Level the playing field: Extend to Start-ups not accessing Govt Funds to start

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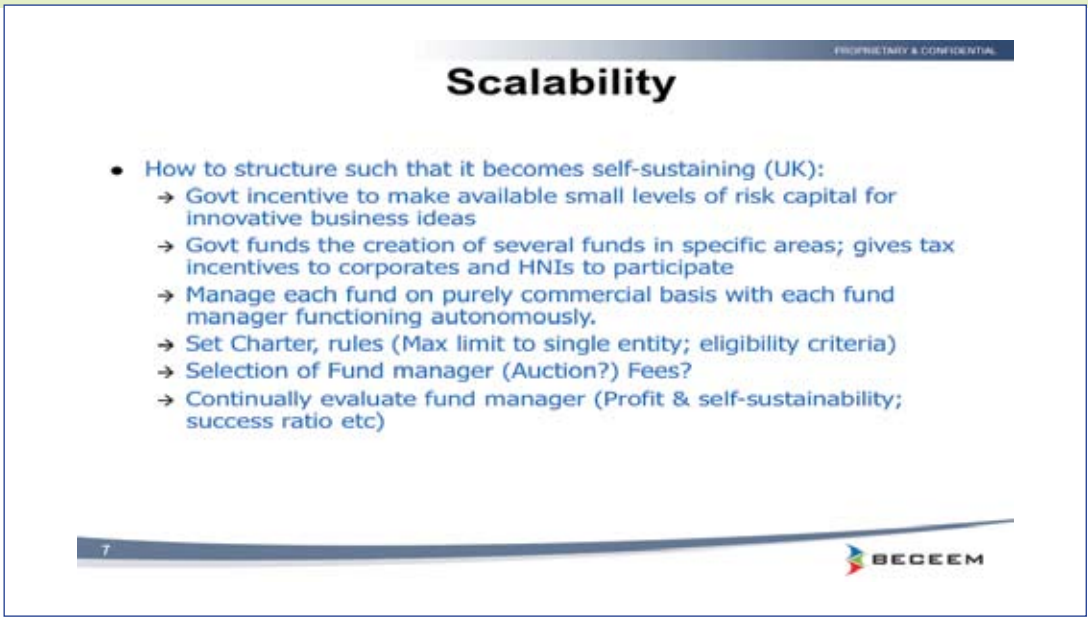
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Scalability
How to structure such that it becomes self-sustaining (UK):
→ Govt incentive to make available small levels of risk capital for innovative business ideas
→ Govt funds the creation of several funds in specific areas; gives tax incentives to corporates and HNIs to participate
→ Manage each fund on purely commercial basis with each fund manager functioning autonomously.
→ Set Charter, rules (Max limit to single entity; eligibility criteria)
→ Selection of Fund manager (Auction?) Fees?
→ Continually evaluate fund manager (Profit & self-sustainability; success ratio etc)
7
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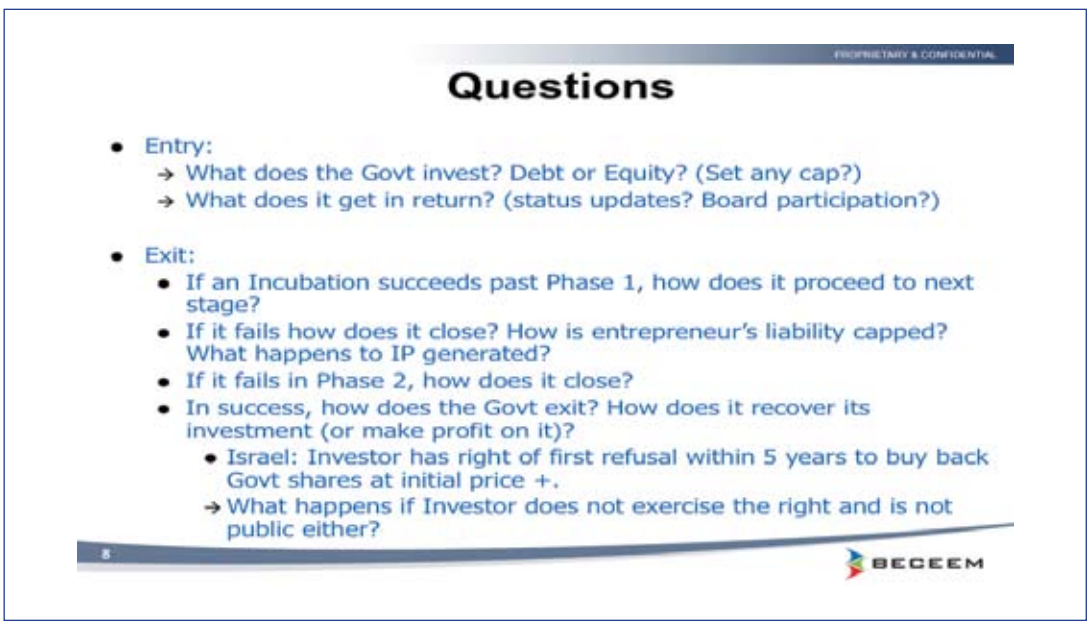
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Questions
Entry:
→ What does the Govt invest? Debt or Equity? (Set any cap?)
→ What does it get in return? (status updates? Board participation?)
Exit:
If an Incubation succeeds past Phase 1, how does it proceed to next stage?
If it fails how does it close? How is entrepreneur's liability capped? What happens to IP generated?
If it fails in Phase 2, how does it close?
In success, how does the Govt exit? How does it recover its investment (or make profit on it)?
Israel: Investor has right of first refusal within 5 years to buy back Govt shares at initial price +.
→ What happens if Investor does not exercise the right and is not public either?
8
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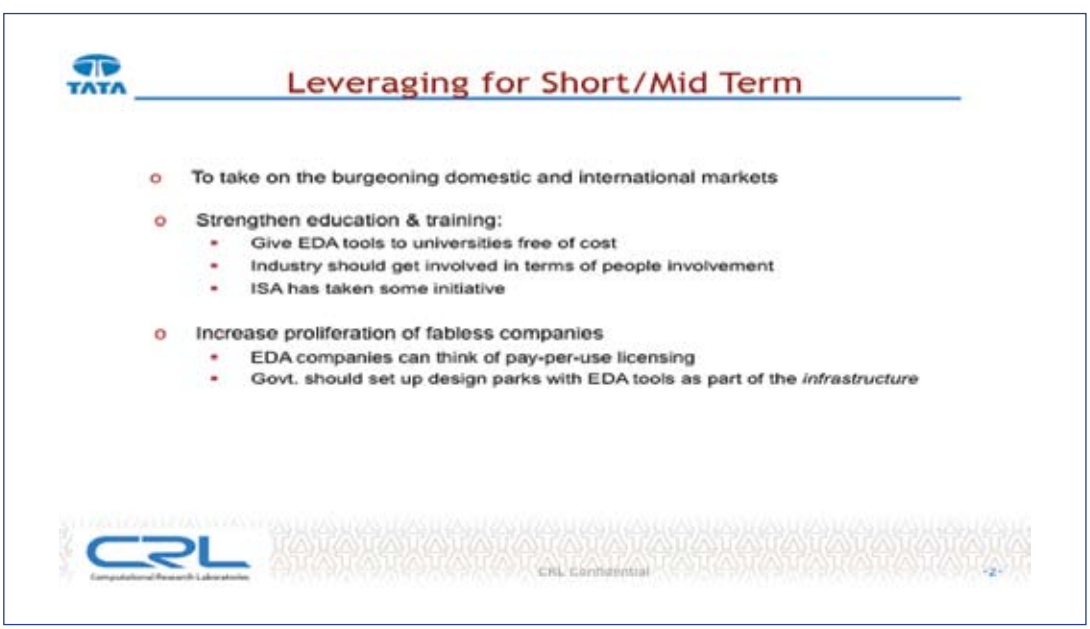
Sunil Sherlekar Founder & Head of Research, Computational Research Labs. Ltd. & Chief Scientist, Tata Consultancy Services Ltd., Bangalore



Sunil Sherlekar Founder & Head of Research, Computational Research Labs. Ltd. & Chief Scientist, Tata Consultancy Services Ltd., Bangalore

Leveraging for Indian Market

- Requirements are:
  - Diverse
  - Smaller volumes per kind of chip
- Set up fabs with older technologies
  - Lower capital and NRE costs: hence cheaper/chip for small volumes
  - Govt. policy should address this

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Leveraging for Long Term

- To take on the world
- Govt. should get more proactive in getting fabs set up in India
  - All creative work will need closer designer-fab interaction, abstractions have to be broken!
  - In any case, a lot of abstractions are breaking down for deep sub-micron technologies
- Address the next-generation fab opportunities
  - Fund, direct and leverage the device & process research going on in academia
  - Need stronger *technical* interaction between industry & academia

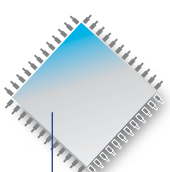
CRL Confidential

Jaswinder Ahuja

Corporate Vice-President and Managing Director,
Cadence Design Systems India Pvt Ltd.

Where are Design Houses?

- India Semiconductor Association Journey with 100+ Members
- Design Ecosystem ; Fab Facility yet to come up
- Many Captive MNC Houses or Indian Design Service Groups---Where are True Design Houses?
- EDA Tool Development exploiting presence of Design Companies in India



Session V : Staircase to Powerhouse

Speakers:

Chandrasekhar
Director, Central Electronics Engineering Research Institute (CEERI), Pilani

Dinesh Sharma
Professor, Indian Institute of Technology, Mumbai

Vivek Pawar
CEO, Sankalp Semiconductor

Ashok Madan
DGM (VLSI/Hardware Division), HCL Technologies Ltd., Noida

Presentations

Staircase to Semiconductor Design Power House

Dr. Chandra Shekhar
Director
CEERI
Pilani – 333 031

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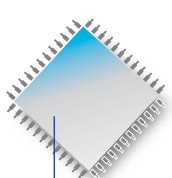
director@ceeri.ernet.in

Staircase Steps

- Step 1 : Quality manpower generation.
- Step 2 : Going beyond chip design.
- Step 3 : Innovative product conceptualization and development.
- Step 4 : Mass manufacture and marketing.

Step 1 : Quality Manpower Generation

- ***Quality*** manpower training on a wider scale.
- Further demystification of VLSI design process and wider deployment of VLSI design tools in academia.
- Push for ME/MTech and PhD students in numbers.



Step 2 : Beyond Chip Design

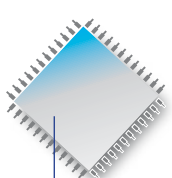
- Wide-scale fab access for chip-prototyping.
- Wide-scale chip-test access.
- Wide-scale access to proto-system/ application development facilities.
- High academic valuation for completion of the complete cycle (chip design, chip prototyping, chip-test, proto-system development).

Step 3 : Innovative Product Conceptualization and Development

- Defining and developing affordable products for the "bottom-of-the-pyramid" population
  - ➢ through *ab-initio* thinking.
  - ➢ leveraging of best technologies to conceive and design products with high performance (say 70% performance *vis-à-vis* the high end products) at disruptively low prices (say 10-15% of the high end products).

Step 4 : Mass Manufacture and Marketing

- On the strength of products described in Step 3, set up manufacturing and marketing — even as we continue providing design services to other global product developers.



Step 1 : Quality Manpower Generation

Current Status

- The two phases of Special Manpower Development Programme (SMDP) of Dept. of IT, Government of India have contributed very significantly to manpower development.

What Further ?

- Cloud Computing (+ licensing) model needed to free academia from the maintenance and upkeep of EDA tools and design environments.

Step 2 : Beyond Chip Design

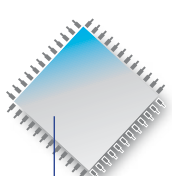
Current Status

- Very few designs go for chip-prototyping. A few of the chips received are tested, and fewer still see use in proto-system development.

Step 2 : Beyond Chip Design

What Further ?

- Facilitate gaining experience of full cycle (chip design, chip-prototype, chip-test, proto-system development and test) by setting up/providing access to chip-testing and proto-system development and test facility centres.
- Build a strong academic emphasis on completion of full cycle and provide valuation/reward for it.
- Learn to value imagination and creativity (needed for product conceptualization and design) on par with analytical ability (needed for providing design services).



Step 3 : Innovative Product Conceptualization and Development

Current Status

- Very little has happened so far.

DST, Govt. of India has set up some generic Technology Incubation Centres (TICs) and the technology Entrepreneurship Promotion Programmes (TEPPs) at some of the academic institutions and R&D labs.

Step 3 : Innovative Product Conceptualization and Development

What Further ?

- Set up focused **Semiconductor Innovation Centres/Parks** with facilities to support the full cycle with easy access to students and young researchers.
- Provide angel funding to student-innovators and young researcher-innovators.

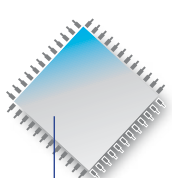
Step 4 : Mass Manufacture and Marketing

Current Status

- We are established players in services but are watching from the side lines on product definition, design and development.

What Further ?

- Let us do what needs to be further done on Steps 1, 2 and 3 and then we would be ready for Step 4.



Semiconductor Design Opportunity Areas

Traditional

- VLSI Design (full spectrum).
- Low Power Design.
- Mixed Signal Design.
- RF Design.
- Compound Semiconductors (GaAs, GaN) based Design.

Semiconductor Design Opportunity Areas

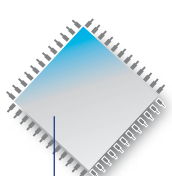
More than Moore

- MEMS Design.
- Sensor Design.
- Signal Conditioning Circuit Design.
- Sensor-electronics Integration.
- Solar Photovoltaics, White LEDs.
- Lasers, Photonics.

Semiconductor Design Opportunity Areas

More than Von Neumann

- Application Specific Processor (ASP) Design.
- Application Specific Instruction Set Processor (ASIP) Design.
- Hardware-Software Co-design.
  (for high performance and low power SoC Design)
- Reconfigurable Computing Systems Design.



Semiconductor Design Opportunity Areas

Future CAD

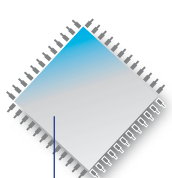
- Upgradation of conventional EDA tools.
- Sub-32 *nm* TCAD tools.
- Analog synthesis tools.
- Mixed signal synthesis tools.
- Next-generation physical design tools.
- Hardware-software co-synthesis tools.

Need for An Indigenous Processor for Strategic Applications

- It is important because it is a wish (in fact, a dream) of the strategic sector who take great pride in self-reliance in matters of advanced technology.
- On a totally professional plane, having a indigenous processor can provide a good platform for building of SoCs, ASPs and ASIPs for low power, high performance, embedded real-time systems.

Way Forward for An Indigenous Processor for Strategic Applications

- Available opensource processors (LeonSPARC, MIPS, OpenSPARC, ...) can be leveraged.
- Linux/RT-Linux can be leveraged.
- Institutionalized (continuing) development approach in PPP mode would be needed with strategic user buying-in upfront.



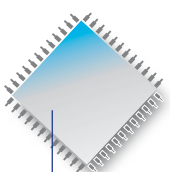
Dinesh Sharma

Professor,
Indian Institute of Technology, Mumbai

Educational Institution

- Strength #1: Excellent Human Capital
- Strength #2: Reasonable Design Infrastructure
- Strength #3: Awareness of Technologies and Design Styles of the Future

- Weakness #1: Poor Access to Test Facilities
- Weakness #2: Low Silicon Experience
- Weakness #3: Inadequate Contact between Industry and Academia
- Weakness # 4: Design Infrastructure Restricted to few Institutions



Developing Talent and Entrepreneurs in Tier II cities

Making India power house for Semiconductor Design

Vivek Pawar
CEO,
Sankalp Semiconductor

1

Critical aspects

- Eco-system
  - Market, Funding, manufacturing, available talent, ...
- Enabling local entrepreneurs
  - Amongst many others Talent Development /Academia is citical

2

Facts / Lessons learned

- Tier II cities growth critical for India's growth
- Chasm in academics and Industry deep
  - All EE students/Profs not capable for semiconductor
  - Any system implemented should be on performance based.
  - Faculty training/Student training be merit based
- Student learning
  - 1 Hr theory and 3 hrs tutorial + practical.
  - Maximum learning on Project

3

Facts / Lessons learned

- Entrepreneurial development needs
  - Low cost R&D
  - Lower cost capital
  - Ready talent at lower cost of ownership
  - Lower cost/risk of idea/innovation evaluation
  - Low/zero cost ready to use infrastructure

4

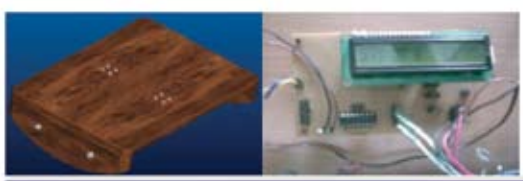
Impact of Industry In Campus

- Year — # of Analog VLSI project
  - 2005 — 0
  - 2009 — 4 + 5 + 1 research
- KRK Rao foundation for Mixed-signal VLSI
  - 4/5 courses were in Hubli due to VLSI infrastructure
  - Selected top 5 profs. Out of total 45+ participants in 3 yrs
  - 4 out of 5 profs from BVB College
  - 2 projects out of 3 to be put on Test chip
- All India Cadence Design contest
  - First time ever 2 entries from same college selected for final round.
  - First prize: IIT Delhi, Second prize: BVB College Hubli

3

Impact of Industry In Campus

- "Walking Tutor", "Eye Trainer" and "Speech and Cognitive Trainer" projects from BVB College, Hubli were the only selection by IEEE international in top 15 academic projects in world
- Stanford's Lab on chip won first prize and second prize went to BVB College
- First time ever!
- Therapeutic Balance Board (TEBB) for mentally challenged kids ready for production and many doctors waiting for product.



6

Proposed model

- Faculty identification/ Ramp up
  - Basic and advanced course followed by product prototype project
  - Certification of excellence certified
- Students ramping up through mini/mega projects
  - UG/PG Diploma faculty/Industry driven
- Industry sponsored
  - Sponsors few projects every year
  - Organization takes responsibility of project execution
- Industry experts as evangelist for project guidance

7

Innovation competition

- Innovation competition with corporate(ISA member) sponsorship.
  - Phased approach and phased rewards/ monetary support
  - Big rewards for working prototypes and successful business plans
  - Hubli experience (TiE, DF)
    - 26 Biz plans -> 16 biz plan mentoring -> Top 10 selected for mentoring -> 5 Successful business in Hubli
- Eligibility
  - Students team with Industry guide and Industry sponsor

8

Eco-system in Tier II cities

- Promote and incentivize Semiconductor companies in Tier II cities
- MNC's can outsource work to Tier II cities
  - Onsite and offsite debate does not have to continue

9

Ashok Madan, DGM (VLSI/Hardware Division), HCL Technologies Ltd., Noida

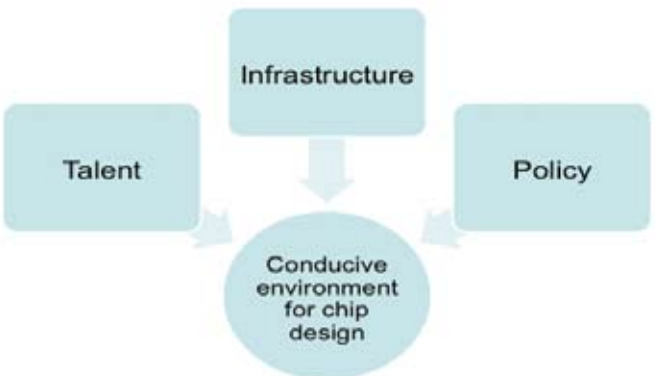
Ashok Madaan
Phone: 9811591089
Email: ashok.madaan@hcl.in

HCL

A Value Leader

HCL

The 3 Enablers



HCL

Importance of Indigenous Chip Design

Uniqueness of Indian market

- Harsh environmental conditions
- Large middle class consuming population
- Huge mass market at very low price points
- Unique consumption patterns due to diverse cultural/ geographic/demographic needs

Strategic – Space/ Defense applications

- Security Concerns
- Privacy Concerns
- Military Applications

Ashok Madan, DGM (VLSI/Hardware Division), HCL Technologies Ltd., Noida

HCL

Feasibility of Indigenous Chip Design

- Irrelevant question as It's already proven
- Some facts and quotes:
  - All the tope 10 semiconductor companies have design centres in India called "India Captives"
  - Gartner
    - These India captives take advantage of the availability of skilled and low-cost workforce to develop products for global markets. *"If these developments are to be done in their respective countries, the development cost will be at least 300% compared to India."*
    - Market for third-party chip design services in India is estimated at about $400 million
    - "Indian design service companies are gaining an increasing share of designs in advanced process nodes. Designs in new process nodes bring with them their own set of challenges but at the same time, as they are cutting-edge.
  - Intel India was responsible for the end-to-end design of Intel's first six-core microprocessor. This is the first time that a microprocessor came to life in a lab in India. Intel had never taken work on 45-nanometer technology outside the US until now. It is also the first time that Intel has released the first design iteration of a chip.
  - India is at the forefront of VLSI design owing to the leading, cutting-edge chip design activities taking place in multinational design companies that have large scale engineering operations here. **Dasaradha Gude,** MD, AMD India

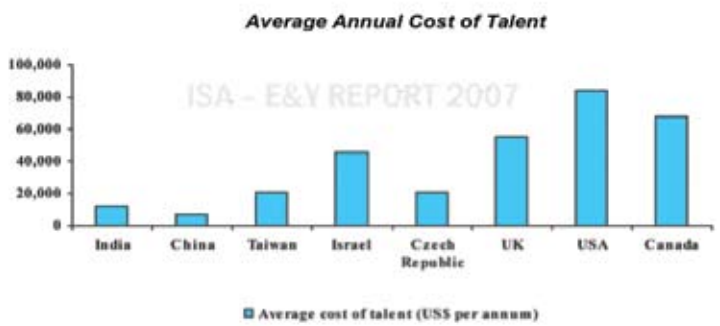
HCL

What Makes India An Attractive Destination

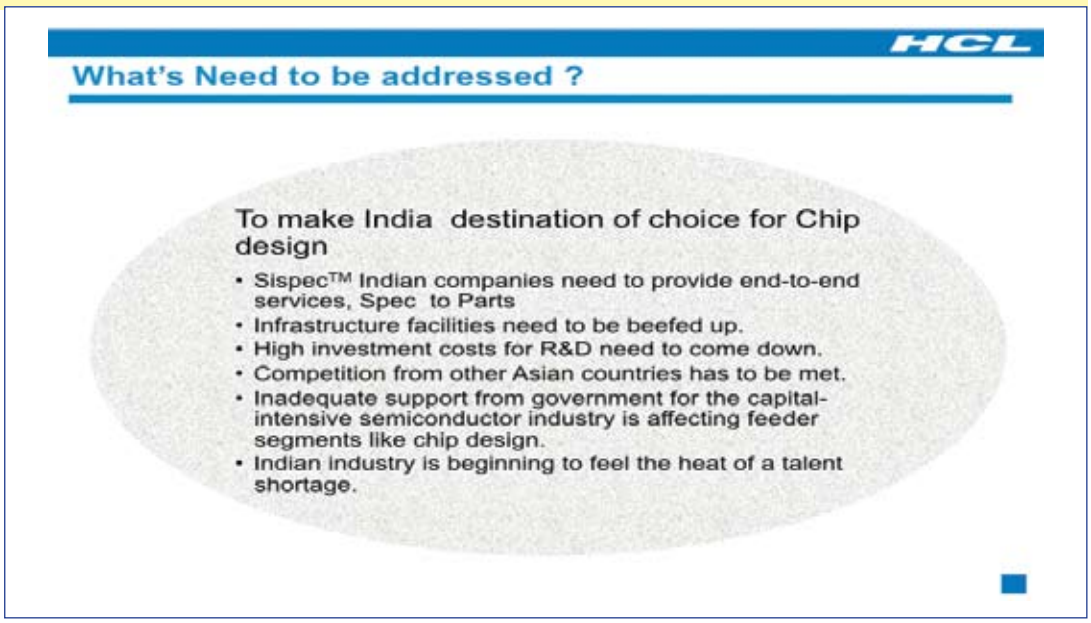
- Positive atmosphere.
- Stable political and robust legal environment
- Emergence of India's services sector, and creation of a technology hub serving the entire globe.
- Advantages of speed and cost in research and development, process development design, project management, etc.
- Highly skilled and cost-effective workforce.
- Respect for Intellectual Property Rights (IPRs): India has a good track record of safeguarding the IPRs of foreign companies, it encourages them to establish design centers in India.
- Emergence of R&D and design centers of homegrown companies, like HCL and Wipro.

HCL

Country Competitiveness: Comparative Talent Cost



Ashok Madan, DGM (VLSI/Hardware Division), HCL Technologies Ltd., Noida



Presentations

Banquet Lecture

Speaker:

Prof. S.K. Brahamachari
DG, CSIR


COVER
Open Source Hardware
Open source hardware could well be India's best bet to get started with a hardware industry, without spending years designing microchips from scratch, writes
CSIR-INDIA
Open Source Beyond Drug Discovery
India Microprocessor Initiative : Team India Effort
Prepared by Dr. J. Bhattacharya, Adjunct Faculty, IIT Delhi
Presented by Prof Brahmachari, DG, CSIR


Chandrayaan - 1
INDIA'S FIRST MISSION TO THE MOON
• To Achieve 100 x 100 km Lunar Polar Orbit.
• PSLV to inject 1050 kg in GTO of 240 x 36000 km.
• Lunar Orbital mass of 523 kg with 2 year lifetime.
• Scientific payload 55 kg.
Lunar Insertion Manoeuvre
Final Orbit 100 km Polar
Lunar Transfer
Initial Orbit
The hand that sent Jupiter spinning through heaven,
Spends all its cunning to fashion a curl
- Sri Aurobindo
GTO
Trans Lunar Injection
Mid Course Correction
Expanding the scientific knowledge about the moon, upgradin
and providing challenging opportunities for planetary research

Social Microelectronics

- In 2000, 1,36,000 mothers died in childbirth - the highest in the world*
  - 1 Maternal Mortality every 7 minutes**
- Almost half of pregnant women do not get any antenatal checkup*
- One million children die every year before they become 28 days old***

*http://www.who.int/features/2004/great_expectations/part1/en/index4.html

**http://articles.timesofindia.indiatimes.com/2009/01/15/Childbirth_One_mother_dies_every_7_mins/

***http://timesofindia.indiatimes.com/India/Childbirth_1_mother_dies_every_7_mins/articleshow/3985176.cms

Prepared by Dr. J. Bhattacharya, Adjunct Faculty, IIT Delhi
Presented by Prof Brahmachari, DG, CSIR

Tremendous technological bottlenecks for Social Infrastructure

- Tele-health
- Non-availability of Rs 10,000 Ultrasound equipment
- Non-availability of Rs 5,000 ECG equipment
- Tele-education
- Intelligent irrigation such as moisture triggered drip irrigation
- Rs 500 mobile phone
- Rs 200 per person Microfinance infrastructure
- Rs 1,000 per household lighting solution

Prepared by Dr. J. Bhattacharya, Adjunct Faculty, IIT Delhi
Presented by Prof Brahmachari, DG, CSIR

Nanonization not happening in IT

- Nano could happen because we owned the automobile technology
- A "nano" in microprocessor related areas cannot happen since ownership of technology is a necessary condition
- Ownership of technology if not a sufficient condition
- Design criteria and priorities for design trade-off need to be India specific
  - Smaller & faster is not an India design priority
  - High temp and dust proof is a India design requirement

Prepared by Dr. J. Bhattacharya, Adjunct Faculty, IIT Delhi
Presented by Prof Brahmachari, DG, CSIR

What about sustainability ?

Technological Sovereignty

- Denial of technology by Motorola
- EOL of Motorola microprocessor
- Refusal by Intel to setup Fab in India
- Setting up of Fab in Hyderabad by SemIndia postponed sine die
- Component industry in India is insignificant
- No IPR control in the IT Industry in India
- Consolidation in the Industry
- Colour TV Technology


India's feeble claims to digital sovereignty

GUEST COLUMN

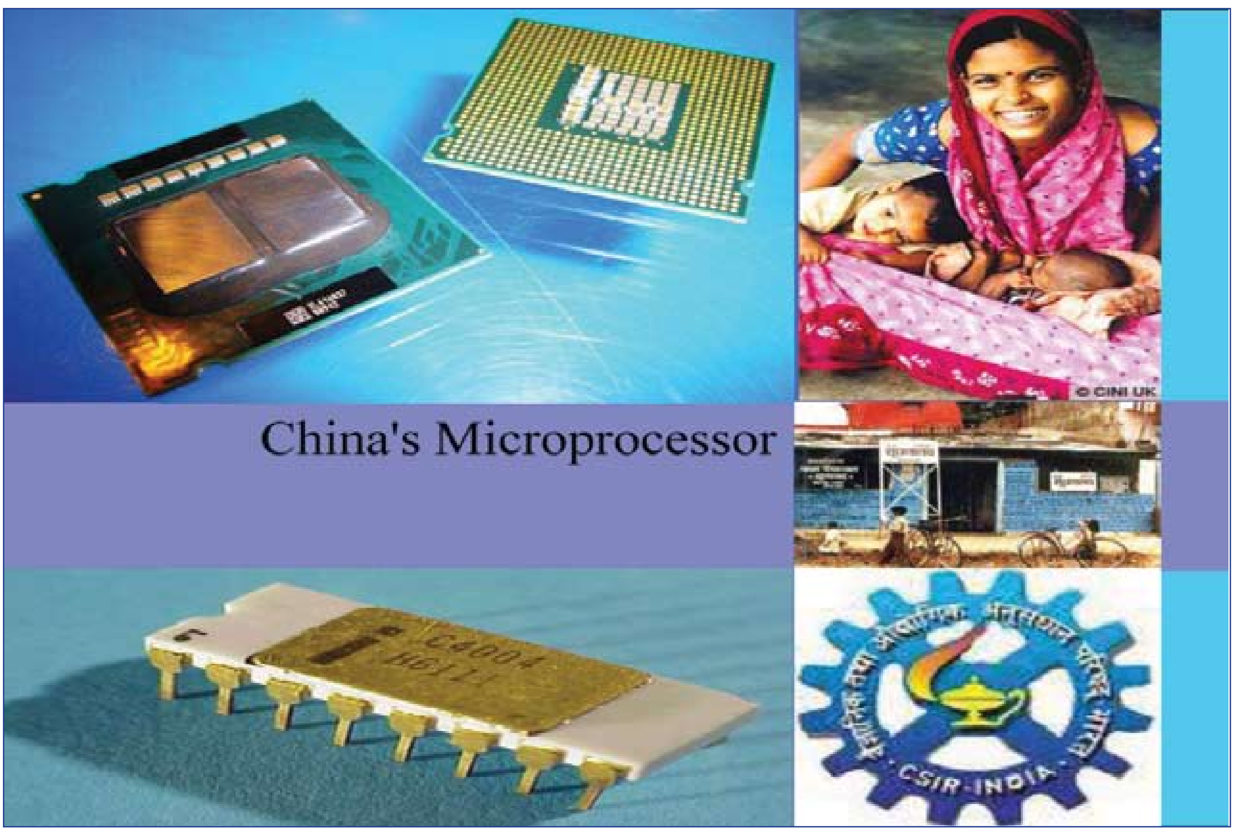
Prepared by Dr. J. Bhattacharya, Adjunct Faculty, IIT Delhi
Presented by Prof Brahmachari, DG, CSIR

- **We lack ownership of Microprocessor design**

Boost to Hardware Industry

- Hardware demand in India for the year 2007-08 was around USD 36 billion
- Only 50% of the hardware is produced locally
  - Within this 50% local production, very large amount of components are importec
  - Total imports is approximately USD 30 billion
- **Economic impact of USD 90 billion**
- Development of skilled manpower and ecosystem which would promote Investment from the private and multinational companies in microelectronics


Strategic Impact
CHINESE EQUIPMENT CO SHORTLISTED BY BSNL FOR Rs 30,000-CR PROJECT SEEN AS SECURITY THREAT
DON'T AWARD CONTRACT TO HUAWEI: IB, MoD
Govt also sets up panel to examine issue of participation of foreign companies, particularly with regard to security related sensitivities in BSNL tenders
DEFENCE MINISTRY REPRESENTATIVES WERE OF THE VIEW THAT HUAWEI HAS BEEN SET UP WITH THE ASSISTANCE OF THE CHINESE ARMY AND HAS A TAINTED PAST
Prepared by Dr. J. Bhattacharya, Adjunct Faculty, IIT Delhi
Presented by Prof Brahmachari, DG, CSIR


China's Microprocessor
© CINI UK
CSIR-INDIA

China's Microprocessor Strategy

- China has developed a dragon chip based on which Rs 10,000 fully-functional laptops are being sold
- The Microprocessor strategy of China can be broadly classified as:
  - Education
  - Research
  - Industry development
- In 3 years, they aim to train 100-150 teacher trainers majored in IC/Electronics per year
- Facilitate teachers to learn and master the world's most up-to-date technology and tools in IC in a short period of time
  - e.g. FPGA, multi-core and multi-thread, etc.

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Presented by Prof Brahmachari, DG, CSIR

Indian Initiatives

- **Public Sector Initiatives**
- CSIR-CEERI, Pilani
- SCL ,Chandigarh (MANAS)
- BARC (16 bit microprocessor)
- Saha Institute (MANAS)

- **Pvt Sector Initiatives**
- MNC's such as Intel, Freescale, Xilinx, Synopsis, TI etc
- Indian firms such as Wipro, L&T Infotech etc
  - Service providers to MNC's

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Presented by Prof Brahmachari, DG, CSIR

Vision

- Create a semiconductor microprocessor hardware technology development and systems manufacturing capability in India in order to boost the hardware industry in India and for India to own a strategic technology
- Focus on ensuring delivery of low cost services to the masses through effective intervention in social microelectronics
  - Health
  - Communication
  - Education
  - Power
  - Agriculture/ Irrigation
  - Energy

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Presented by Prof Brahmachari, DG, CSIR

Open Source Microprocessor

- Adopting an open source microprocessor core that would allow a low cost acquisition of the strategic microprocessor technology. This will substantially reduce the initial investments in research and development
- Taken forward as Zerone Microsystems

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Presented by Prof Brahmachari, DG, CSIR

Be the change you want to see in the world – Mahatma Gandhi

- CSIR Initiative facilitated by CSIR -CEERI ,Pilani
- Workshop on India Microprocessor Initiative, IIT Delhi
- Ongoing dialogue with Chairman, ISRO
- Coordinating with Ministry of Communication and Information Technology, led by Secretary IT
- Supported by MAIT
- Supported by professors from IIT Delhi and IIM Ahmedabad
- India Microprocessor portal - www.indiamicroprocessor.org
- India Microprocessor mailing group - indiamicroprocessor@yahoogroups.co.in
- In principle willingness to fund this initiative from Tempus Capital and Tallwood Venture Capital
- CSIR has moved through CSIR GB & Planning Commission

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Presented by Prof Brahmachari, DG, CSIR

Unity is Strength - Panchatantra

- Participation from various private sector players and written letters from over 8 private organizations to support this initiative
  - Ncore Technologies (producer of world's first open source handheld computer – Simputer, Bangalore)
  - VirtualWire (IIT Delhi)
  - Synposis (Bangalore)
  - Da Vinci Designs (Bangalore)
  - Nevis Networks (Pune)
  - Concept2Silicon (Bangalore)
  - CoWare Processors (Noida)
  - Calypto Systems (Noida)

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Presented by Prof Brahmachari, DG, CSIR

Prepared by Dr. J. Bhattacharya, Adjunct Faculty, IIT I
Presented by Prof Brahmachari, DG, CSIR

Join the Change You Want to see in Indian IT Hardware

Join the Zerone initiative

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